8-Bit, 40/80/100 MSPS Dual A/D Converter

AD9288

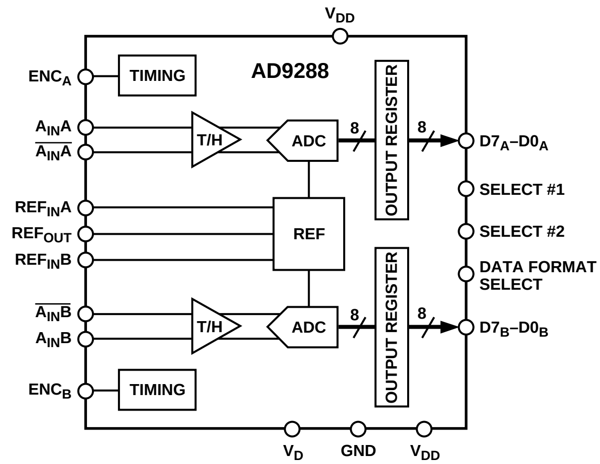
FEATURES

Dual 8-Bit, 40 MSPS, 80 MSPS, and 100 MSPS ADC
Low Power: 90 mW at 100 MSPS per Channel
On-Chip Reference and Track/Holds
475 MHz Analog Bandwidth Each Channel
SNR = 47 dB @ 41 MHz
1 V p-p Analog Input Range Each Channel
Single +3.0 V Supply Operation (2.7 V–3.6 V)
Standby Mode for Single Channel Operation
Twos Complement or Offset Binary Output Mode
Output Data Alignment Mode

APPLICATIONS

Battery Powered Instruments
Hand-Held Scopemeters
Low Cost Digital Oscilloscopes
I and Q Communications

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9288 is a dual 8-bit monolithic sampling analog-to-digital converter with on-chip track-and-hold circuits and is optimized for low cost, low power, small size and ease of use. The product operates at a 100 MSPS conversion rate with outstanding dynamic performance over its full operating range. Each channel can be operated independently.

The ADC requires only a single 3.0 V (2.7 V to 3.6 V) power supply and an encode clock for full-performance operation. No external reference or driver components are required for many applications. The digital outputs are TTL/CMOS compatible and a separate output power supply pin supports interfacing with 3.3 V or 2.5 V logic.

The encode input is TTL/CMOS compatible and the 8-bit digital outputs can be operated from +3.0 V (2.5 V to 3.6 V) supplies. User-selectable options are available to offer a combination of standby modes, digital data formats and digital data timing schemes. In standby mode, the digital outputs are driven to a high impedance state.

Fabricated on an advanced CMOS process, the AD9288 is available in a 48-lead surface mount plastic package (7 × 7 mm, 1.4 mm LQFP) specified over the industrial temperature range (–40°C to +85°C).

REV. 0

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AD9288–SPECIFICATIONS (V_{DD} = 3.0 V; V_D = 3.0 V, Differential Input; External reference unless otherwise noted.)

Parameter	Temp	Test Level	AD9288BST-100 Min	AD9288BST-100 Typ	AD9288BST-100 Max	AD9288BST-80 Min	AD9288BST-80 Typ	AD9288BST-80 Max	AD9288BST-40 Min	AD9288BST-40 Typ	AD9288BST-40 Max	Units
RESOLUTION				8			8			8		Bits
DC ACCURACY												
Differential Nonlinearity	+25°C	I		±0.5	+1.25		±0.5	+1.25		±0.5	+1.25	LSB
	Full	VI			+1.50			+1.50			+1.50	LSB
Integral Nonlinearity	+25°C	I		±0.50	+1.25		±0.50	+1.25		±0.50	+1.25	LSB
	Full	VI			+1.50			+1.50			+1.50	LSB
No Missing Codes	Full	VI		Guaranteed			Guaranteed			Guaranteed		
Gain Error[1]	+25°C	I	–6	±2.5	+6	–6	±2.5	+6	–6	±2.5	+6	% FS
	Full	VI	–8		+8	–8		+8	–8		+8	% FS
Gain Tempco[1]	Full	VI		80			80			80		ppm/°C
Gain Matching	+25°C	V		±1.5			±1.5			±1.5		% FS
Voltage Matching	+25°C	V		±15			±15			±15		mV
ANALOG INPUT												
Input Voltage Range (With Respect to $\overline{A_{IN}}$)	Full	V		±512			±512			±512		mV p-p
Common-Mode Voltage	Full	V		±200			±200			±200		mV
Input Offset Voltage	+25°C	I	–35	±10	+35	–35	±10	+35	–35	±10	+35	mV
	Full	VI		±40			±40			±40		mV
Reference Voltage	Full	VI	1.2	1.25	1.3	1.2	1.25	1.3	1.2	1.25	1.3	V
Reference Tempco	Full	VI		±130			±130			±130		ppm/°C
Input Resistance	+25°C	I	7	10	13	7	10	13	7	10	13	kΩ
	Full	VI	5		16	5		16	5		16	kΩ
Input Capacitance	+25°C	V		2			2			2		pF
Analog Bandwidth, Full Power	+25°C	V		475			475			475		MHz
SWITCHING PERFORMANCE												
Maximum Conversion Rate	Full	VI	100			80			40			MSPS
Minimum Conversion Rate	+25°C	IV			1			1			1	MSPS
Encode Pulsewidth High (t_{EH})	+25°C	IV	4.3		1000	5.0		1000	8.0		1000	ns
Encode Pulsewidth Low (t_{EL})	+25°C	IV	4.3		1000	5.0		1000	8.0		1000	ns
Aperture Delay (t_A)	+25°C	V		0			0			0		ns
Aperture Uncertainty (Jitter)	+25°C	V		5			5			5		ps rms
Output Valid Time (t_V)[2]	Full	VI		3.0			3.0			3.0		ns
Output Propagation Delay (t_{PD})[2]	Full	VI		4.5			4.5			4.5		ns
DIGITAL INPUTS												
Logic "1" Voltage	Full	VI	2.0			2.0			2.0			V
Logic "0" Voltage	Full	VI			0.8			0.8			0.8	V
Logic "1" Current	Full	VI			±1			±1			±1	µA
Logic "0" Current	Full	VI			±1			±1			±1	µA
Input Capacitance	+25°C	V		2.0			2.0			2.0		pF
DIGITAL OUTPUTS[3]												
Logic "1" Voltage	Full	VI	2.45			2.45			2.45			V
Logic "0" Voltage	Full	VI			0.05			0.05			0.05	V
POWER SUPPLY												
Power Dissipation[4]	Full	VI		180	218		171	207		156	189	mW
Standby Dissipation[4, 5]	Full	VI		6	11		6	11		6	11	mW
Power Supply Rejection Ratio (PSRR)	+25°C	I		8	20		8	20		8	20	mV/V
DYNAMIC PERFORMANCE[6]												
Transient Response	+25°C	V		2			2			2		ns
Overvoltage Recovery Time	+25°C	V		2			2			2		ns
Signal-to-Noise Ratio (SNR) (Without Harmonics)												
f_{IN} = 10.3 MHz	+25°C	I		47.5			47.5		44	47.5		dB
f_{IN} = 26 MHz	+25°C	I		47.5		44	47					dB
f_{IN} = 41 MHz	+25°C	I	44	47.0								dB

Parameter	Temp	Test Level	AD9288BST-100 Min	Typ	Max	AD9288BST-80 Min	Typ	Max	AD9288BST-40 Min	Typ	Max	Units
DYNAMIC PERFORMANCE[6] (Continued)												
Signal-to-Noise Ratio (SINAD) (With Harmonics)												
f_{IN} = 10.3 MHz	+25°C	I		47			47		44	47		dB
f_{IN} = 26 MHz	+25°C	I		47		44	47					dB
f_{IN} = 41 MHz	+25°C	I	44	47			47					dB
Effective Number of Bits												
f_{IN} = 10.3 MHz	+25°C	I		7.5			7.5		7.0	7.5		Bits
f_{IN} = 26 MHz	+25°C	I		7.5		7.0	7.5					Bits
f_{IN} = 41 MHz	+25°C	I	7.0	7.5			7.5					Bits
2nd Harmonic Distortion												
f_{IN} = 10.3 MHz	+25°C	I		70			70		55	70		dBc
f_{IN} = 26 MHz	+25°C	I		70		55	70					dBc
f_{IN} = 41 MHz	+25°C	I	55	70			70					dBc
3rd Harmonic Distortion												
f_{IN} = 10.3 MHz	+25°C	I		60			60		55	60		dBc
f_{IN} = 26 MHz	+25°C	I		60		55	60					dBc
f_{IN} = 41 MHz	+25°C	I	52	60			60					dBc
Two-Tone Intermod Distortion (IMD)												
f_{IN} = 10.3 MHz	+25°C	V		60			60			60		dBc

NOTES

[1]Gain error and gain temperature coefficient are based on the ADC only (with a fixed 1.25 V external reference).

[2]t_V and t_{PD} are measured from the 1.5 V level of the ENCODE input to the 10%/90% levels of the digital outputs swing. The digital output load during test is not to exceed an ac load of 10 pF or a dc current of ±40 µA.

[3]Digital supply current based on V_{DD} = +3.0 V output drive with <10 pF loading under dynamic test conditions.

[4]Power dissipation measured under the following conditions: f_S = 100 MSPS, analog input is –0.7 dBFS, both channels in operation.

[5]Standby dissipation calculated with encode clock in operation.

[6]SNR/harmonics based on an analog input voltage of –0.7 dBFS referenced to a 1.024 V full-scale input range.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_D, V_{DD} . . . . +4 V
Analog Inputs . . . . –0.5 V to V_D + 0.5 V
Digital Inputs . . . . –0.5 V to V_{DD} + 0.5 V
VREF IN . . . . –0.5 V to V_D + 0.5 V
Digital Output Current . . . . 20 mA
Operating Temperature . . . . –55°C to +125°C
Storage Temperature . . . . –65°C to +150°C
Maximum Junction Temperature . . . . +175°C
Maximum Case Temperature . . . . +150°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Ranges	Package Options
AD9288BST -40, -80, -100	–40°C to +85°C	ST-48*
AD9288/PCB	+25°C	Evaluation Board

*ST = Thin Plastic Quad Flatpack (1.4 mm thick, 7 × 7 mm: LQFP).

EXPLANATION OF TEST LEVELS

Test Level

I 100% production tested.

II 100% production tested at +25°C and sample tested at specified temperatures.

III Sample tested only.

IV Parameter is guaranteed by design and characterization testing.

V Parameter is a typical value only.

VI 100% production tested at +25°C; guaranteed by design and characterization testing for industrial temperature range; 100% production tested at temperature extremes for military devices.

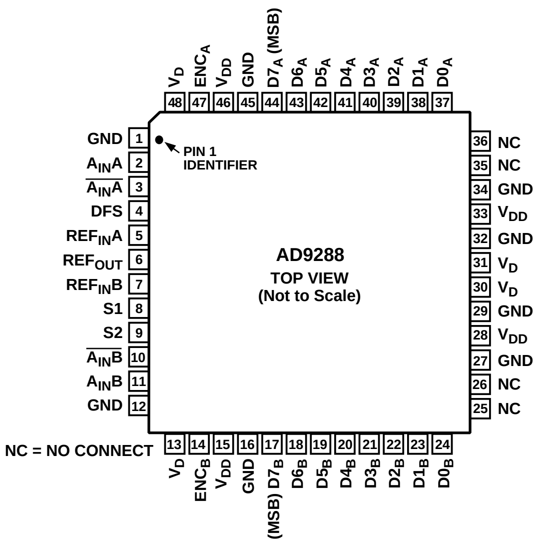
Table I. User Select Options

S1	S2	User Select Options
0	0	Standby Both Channels A and B.
0	1	Standby Channel B Only.
1	0	Normal Operation (Data Align Disabled).
1	1	Data align enabled (data from both channels available on rising edge of Clock A. Channel B data is delayed a 1/2 clock cycle).

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9288 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Name	Description
1, 12, 16, 27, 29, 32, 34, 45	GND	Ground.
2	$A_{IN}A$	Analog Input for Channel A.
3	$\overline{A_{IN}A}$	Analog Input for Channel A (Complementary).
4	DFS	Data Format Select: (Offset binary output available if set low. Twos complement output available if set high).
5	$REF_{IN}A$	Reference Voltage Input for Channel A.
6	REF_{OUT}	Internal Reference Voltage.
7	$REF_{IN}B$	Reference Voltage Input for Channel B.
8	S1	User Select #1 (Refer to Table I), Tied with Respect to V_D.
9	S2	User Select #2 (Refer to Table I), Tied with Respect to V_D.
10	$\overline{A_{IN}B}$	Analog Input for Channel B (Complementary).
11	$A_{IN}B$	Analog Input for Channel B.
13, 30, 31, 48	V_D	Analog Supply (3 V).
14	ENC_B	Clock Input for Channel B.
15, 28, 33, 46	V_{DD}	Digital Supply (3 V).
17–24	$D7_B$–$D0_B$	Digital Output for Channel B.
25, 26, 35, 36	NC	Do Not Connect.
37–44	$D0_A$–$D7_A$	Digital Output for Channel A.
47	ENC_A	Clock Input for Channel A.

DEFINITION OF SPECIFICATIONS

Analog Bandwidth (Small Signal)
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between a differential crossing of ENCODE and $\overline{\text{ENCODE}}$ and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Differential Nonlinearity
The deviation of any code from an ideal 1 LSB step.

Encode Pulsewidth/Duty Cycle
Pulsewidth high is the minimum amount of time that the ENCODE pulse should be left in Logic "1" state to achieve rated performance; pulsewidth low is the minimum time ENCODE pulse should be left in low state. At a given clock rate, these specs define an acceptable Encode duty cycle.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least square curve fit.

Minimum Conversion Rate
The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate
The encode rate at which parametric testing is performed.

Output Propagation Delay
The delay between a differential crossing of ENCODE and $\overline{\text{ENCODE}}$ and the time when all output data bits are within valid logic levels.

Power Supply Rejection Ratio
The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise-and-Distortion (SINAD)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics but excluding dc.

Signal-to-Noise Ratio (SNR)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

Spurious-Free Dynamic Range (SFDR)
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. May be reported in dBc (i.e., degrades as signal levels is lowered), or in dBFS (always related back to converter full scale).

Two-Tone Intermodulation Distortion Rejection
The ratio of the rms value of either input tone to the rms value of the worst third order intermodulation product; reported in dBc.

Two-Tone SFDR
The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. May be reported in dBc (i.e., degrades as signal levels is lowered), or in dBFS (always related back to converter full scale).

Worst Harmonic
The ratio of the rms signal amplitude to the rms value of the worst harmonic component, reported in dBc.

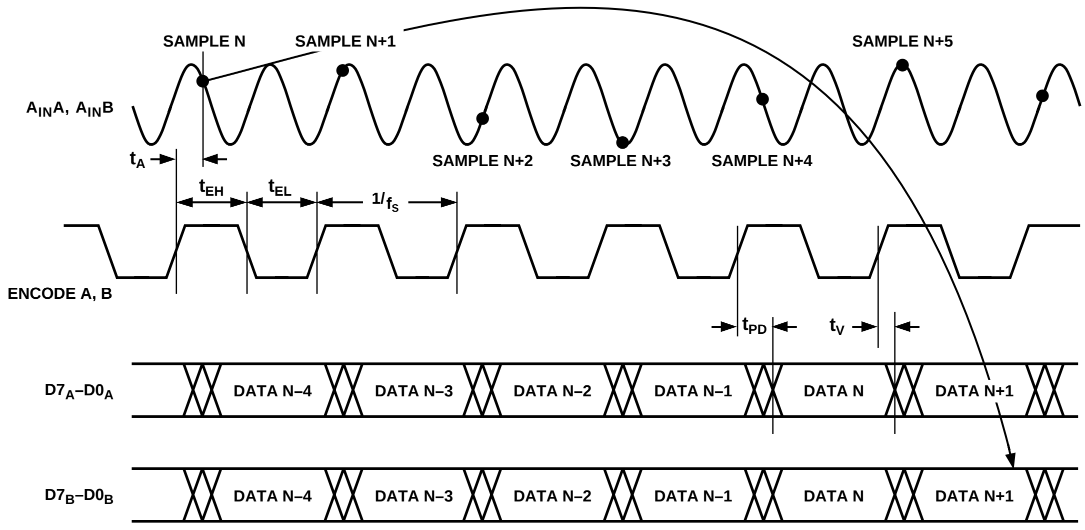


Figure 1. Normal Operation, Same Clock (S1 = 1, S2 = 0) Channel Timing

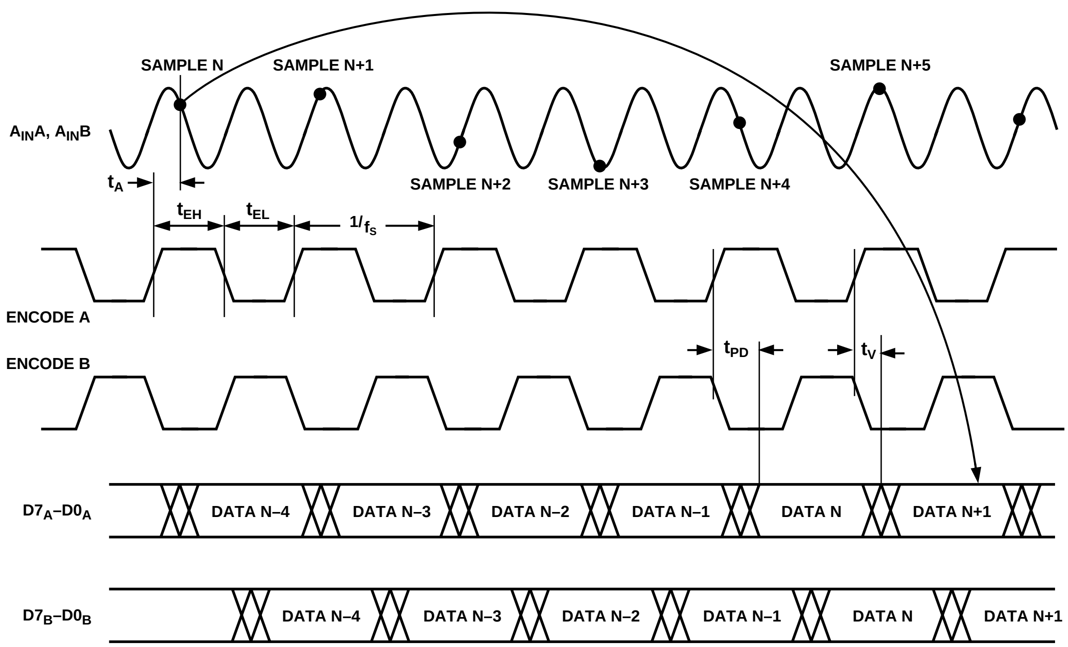


Figure 2. Normal Operation with Two Clock Sources (S1 = 1, S2 = 0) Channel Timing

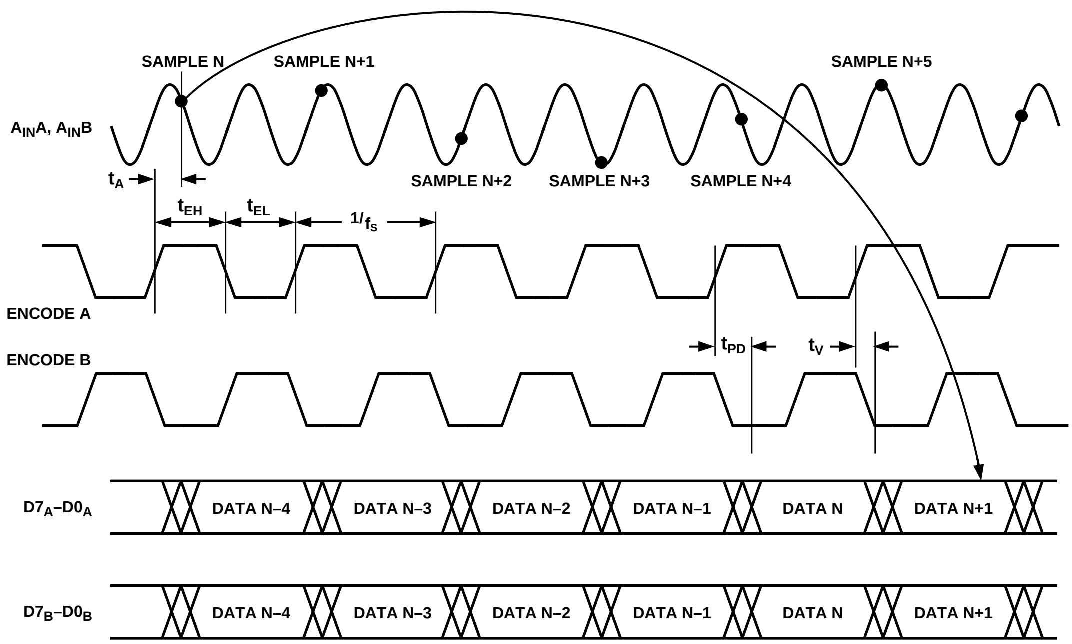


Figure 3. Data Align with Two Clock Sources (S1 = 1, S2 = 1) Channel Timing

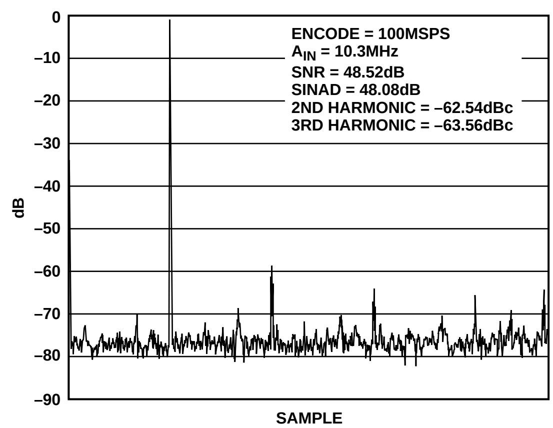


Figure 4. Spectrum: f_S = 100 MSPS, f_{IN} = 10 MHz, Single-Ended Input

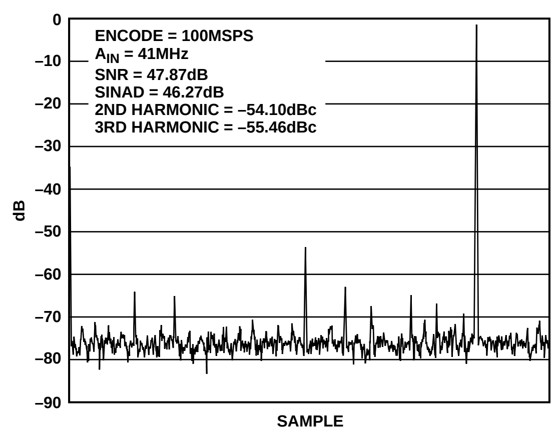


Figure 5. Spectrum: f_S = 100 MSPS, f_{IN} = 41 MHz, Single-Ended Input

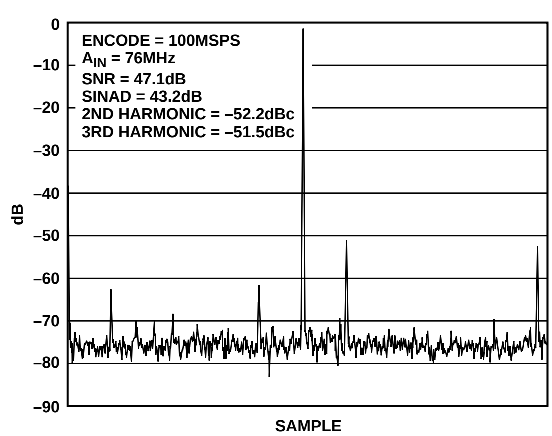


Figure 6. Spectrum: f_S = 100 MSPS, f_{IN} = 76 MHz, Single-Ended Input

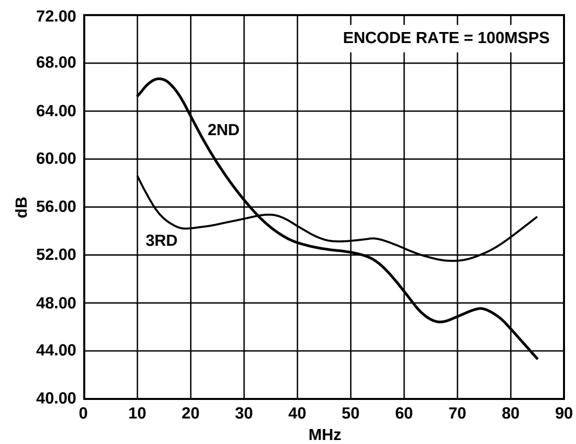


Figure 7. Harmonic Distortion vs. A_{IN} Frequency

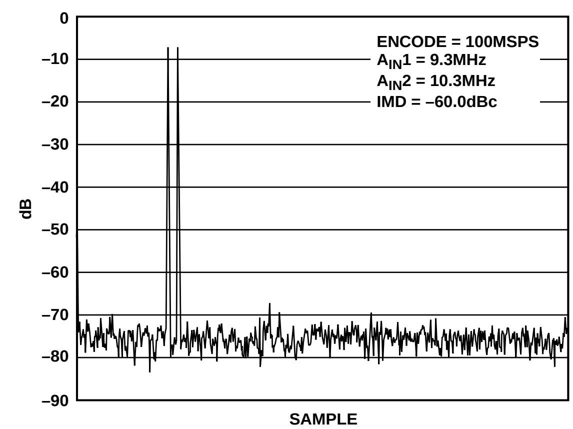


Figure 8. Two-Tone Intermodulation Distortion

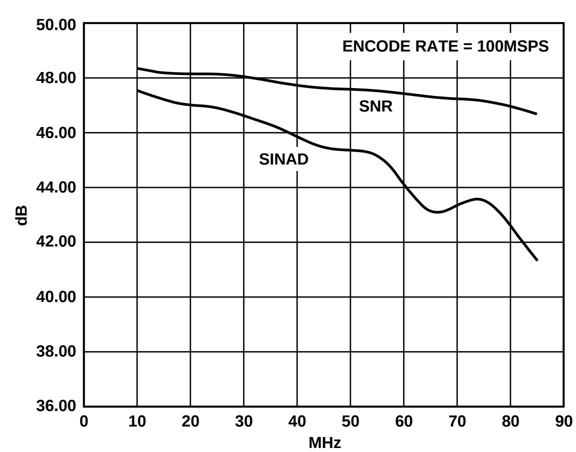


Figure 9. SINAD/SNR vs. A_{IN} Frequency

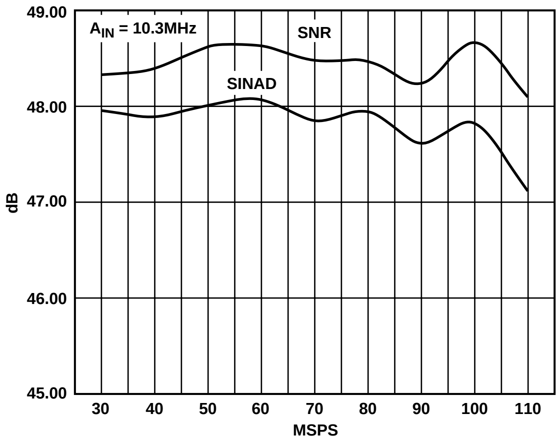


Figure 10. SINAD/SNR vs. Encode Rate

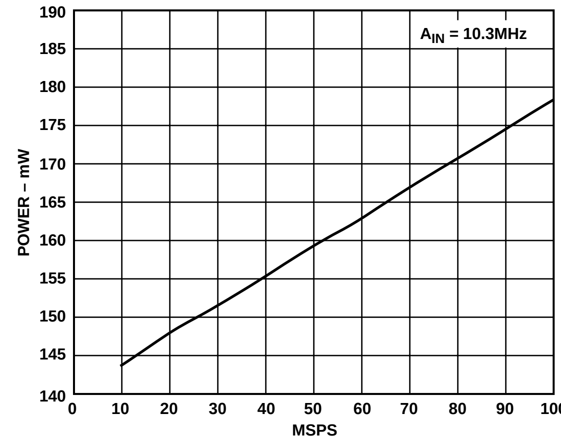


Figure 13. Analog Power Dissipation vs. Encode Rate

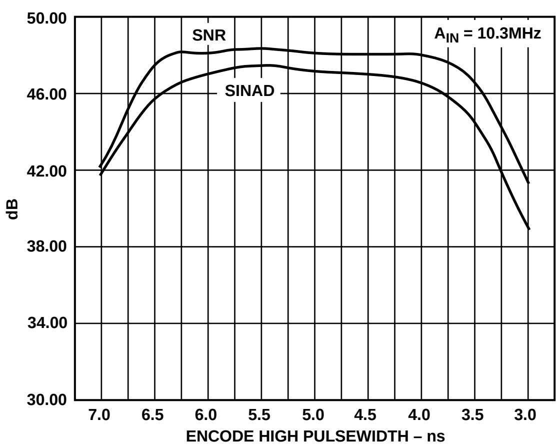


Figure 11. SINAD/SNR vs. Encode Pulsewidth High

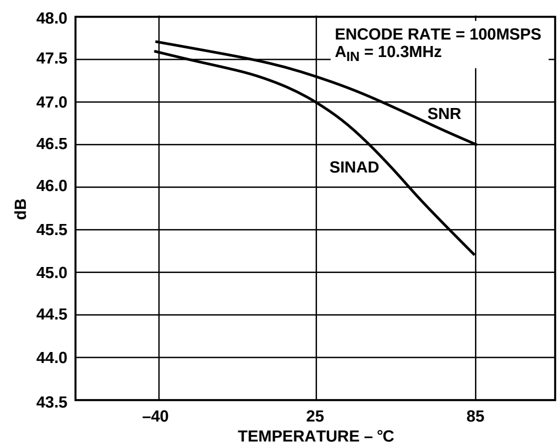


Figure 14. SINAD/SNR vs. Temperature

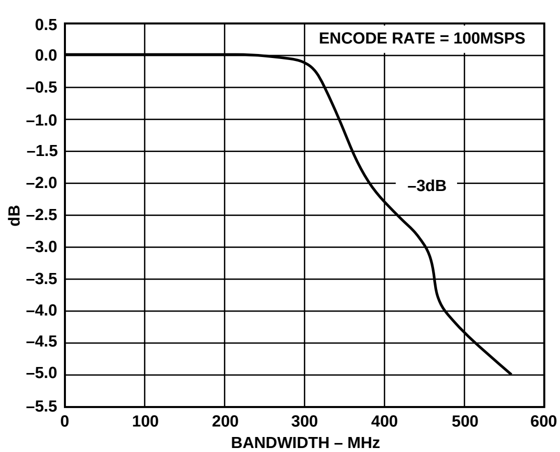


Figure 12. ADC Frequency Response: f_S = 100 MSPS

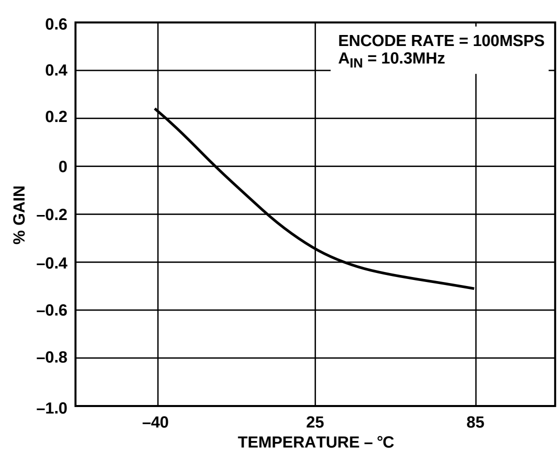


Figure 15. ADC Gain vs. Temperature (with External +1.25 V Reference)

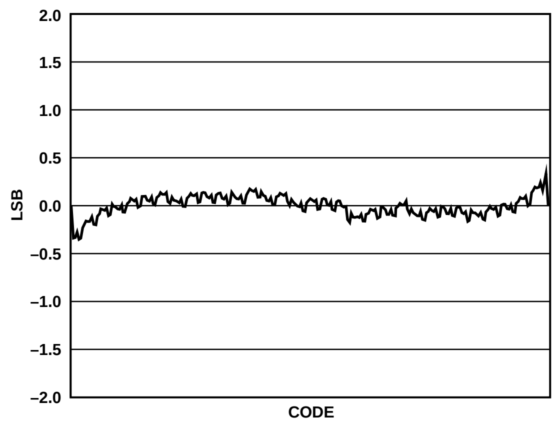


Figure 16. Integral Nonlinearity

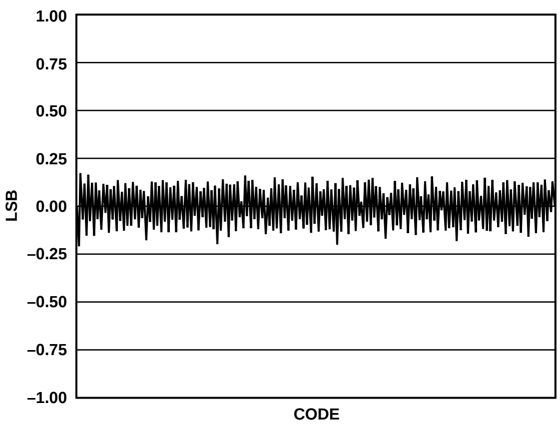


Figure 17. Differential Nonlinearity

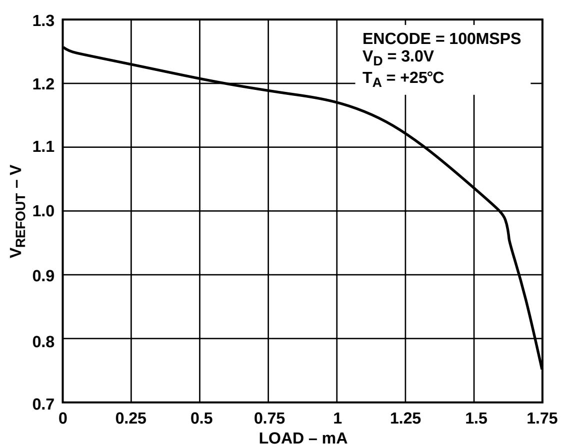


Figure 18. Voltage Reference Out vs. Current Load

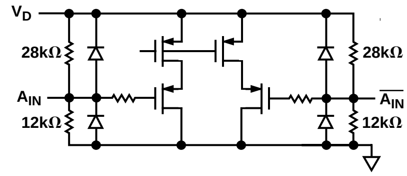


Figure 19. Equivalent Analog Input Circuit

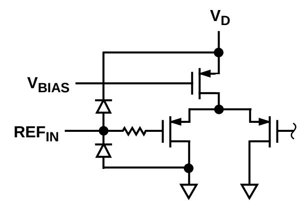


Figure 20. Equivalent Reference Input Circuit

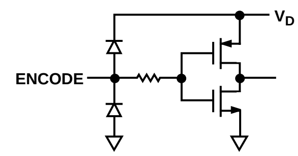


Figure 21. Equivalent Encode Input Circuit

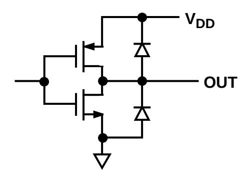


Figure 22. Equivalent Digital Output Circuit

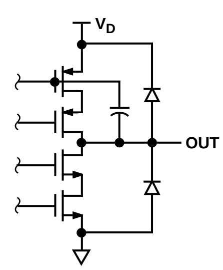


Figure 23. Equivalent Reference Output Circuit

APPLICATION NOTES

THEORY OF OPERATION

The AD9288 ADC architecture is a bit-per-stage pipeline-type converter utilizing switch capacitor techniques. These stages determine the 5 MSBs and drive a 3-bit flash. Each stage provides sufficient overlap and error correction allowing optimization of comparator accuracy. The input buffers are differential and both sets of inputs are internally biased. This allows the most flexible use of ac or dc and differential or single-ended input modes. The output staging block aligns the data, carries out the error correction and feeds the data to output buffers. The set of output buffers are powered from a separate supply, allowing adjustment of the output voltage swing. There is no discernible difference in performance between the two channels.

USING THE AD9288

Good high speed design practices must be followed when using the AD9288. To obtain maximum benefit, decoupling capacitors should be physically as close to the chip as possible, minimizing trace and via inductance between chip pins and capacitor (0603 surface mount caps are used on the AD9288/PCB evaluation board). It is recommended to place a 0.1 µF capacitor at each power-ground pin pair for high frequency decoupling, and include one 10 µF capacitor for local low frequency decoupling. The VREF IN pin should also be decoupled by a 0.1 µF capacitor. It is also recommended to use a split power plane and contiguous ground plane (see evaluation board section). Data output traces should be short (<1 inch), minimizing on-chip noise at switching.

ENCODE Input

Any high speed A/D converter is extremely sensitive to the quality of the sampling clock provided by the user. A track/hold circuit is essentially a mixer. Any noise, distortion or timing jitter on the clock will be combined with the desired signal at the A/D output. For that reason, considerable care has been taken in the design of the ENCODE input of the AD9288, and the user is advised to give commensurate thought to the clock source. The ENCODE input is fully TTL/CMOS compatible.

Digital Outputs

The digital outputs are TTL/CMOS compatible for lower power consumption. During standby, the output buffers transition to a high impedance state. A data format selection option supports either twos complement (set high) or offset binary output (set low) formats.

Analog Input

The analog input to the AD9288 is a differential buffer. For best dynamic performance, impedance at A_{IN} and $\overline{A_{IN}}$ should match. Special care was taken in the design of the analog input stage of the AD9288 to prevent damage and corruption of data when the input is overdriven. The nominal input range is 1.024 V p-p centered at $V_D \times 0.3$.

Voltage Reference

A stable and accurate 1.25 V voltage reference is built into the AD9288 (REF_{OUT}). In normal operation, the internal reference is used by strapping Pins 5 ($REF_{IN}A$) and 7 ($REF_{IN}B$) to Pin 6 (REF_{OUT}). The input range can be adjusted by varying the reference voltage applied to the AD9288. No appreciable degradation in performance occurs when the reference is adjusted ±5%. The full-scale range of the ADC tracks reference voltage, which changes linearly.

Timing

The AD9288 provides latched data outputs, with four pipeline delays. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the encode command (see Figures 1, 2 and 3). The length of the output data lines and loads placed on them should be minimized to reduce transients within the AD9288. These transients can detract from the converter's dynamic performance.

The minimum guaranteed conversion rate of the AD9288 is 1 MSPS. At clock rates below 1 MSPS, dynamic performance will degrade. Typical power-up recovery time after standby mode is 15 clock cycles.

User Select Options

Two pins are available for a combination of operational modes. These options allow the user to place both channels in standby, excluding the reference, or just the B channel. Both modes place the output buffers and clock inputs in high impedance states.

The other option allows the user to skew the B channel output data by 1/2 a clock cycle. In other words, if two clocks are fed to the AD9288 and are 180° out of phase, enabling the data align will allow Channel B output data to be available at the rising edge of Clock A. If the same encode clock is provided to both channels and the data align pin is enabled, then output data from Channel B will be 180° out of phase with respect to Channel A. If the same encode clock is provided to both channels and the data align pin is disabled, then both outputs are delivered on the same rising edge of the clock.

EVALUATION BOARD

The AD9288 evaluation board offers an easy way to test the AD9288. It provides a means to drive the analog inputs single-endedly or differentially. The two encode clocks are easily accessible at on-board SMB connectors J2, J7. These clocks are buffered on the board to provide the clocks for an on-board DAC and latches. The digital outputs and output clocks are available at a standard 37-pin connector, P2. The board has several different modes of operation, and is shipped in the following configuration:

- Single-Ended Analog Input
- Normal Operation Timing Mode
- Internal Voltage Reference

Power Connector

Power is supplied to the board via a detachable 6-pin power strip, P1.

VREFA	–	Optional External Reference Input	(1.25 V/1 µA)
VREFB	–	Optional External Reference Input	(1.25 V/1 µA)
VDL	–	Supply for Support Logic and DAC	(3 V/215 mA)
VDD	–	Supply for ADC Outputs	(3 V/15 mA)
VD	–	Supply for ADC Analog	(3 V/30 mA)

Analog Inputs

The evaluation board accepts a 1 V analog input signal centered at ground at each analog input. These can be single-ended signals using SMB connectors J5 (channel A) and J1 (Channel B). In this mode use jumpers E4–E5 and E6–E7. (E1–E2 and E9–E10 jumpers should be lifted.)

Differential analog inputs use SMB connectors J4 and J6. Input is 1 V centered at ground. The single-ended input is converted to differential by transformers T1, T2—allowing the ADC performance for differential inputs to be measured using a single-ended source. In this mode use jumpers E1–E2, E3–E4, E7–E8 and E9–E10. (E4–E5 and E6–E7 jumpers should be lifted.)

Each analog input is terminated on the board with 50 Ω to ground. Each input is ac-coupled on the board through a 0.1 µF capacitor to an on-chip resistor divider that provides dc bias. Note that the inverting analog inputs are terminated on the board with 25 Ω (optimized for single-ended operation). When driving the board differentially these resistors can be changed to 50 Ω to provide balanced inputs.

Encode

The encode clock for channel A uses SMB connector J7. Channel B encode is at SMB connector J2. Each clock input is terminated on the board with 50 Ω to ground. The input clocks are fed directly to the ADC and to buffers U5, U6 which drive the DAC and latches. The clock inputs are TTL compatible, but should be limited to a maximum of V_D.

Voltage Reference

The AD9288 has an internal 1.25 V voltage reference. An external reference for each channel may be employed instead. The evaluation board is configured for the internal reference (use jumpers E18–E41 and E17–E19. To use external references, connect to VREFA and VREFB pins on the power connector P1 and use jumpers E20–E18 and E21–E19.

Normal Operation Mode

In this mode both converters are clocked by the same encode clock; latency is four clock cycles (see timing diagram). Signal S1 (Pin 8) is held high and signal S2 (Pin 9) is held low. This is set at jumpers E22–E29 and E26–E23.

Data Align Mode

In this mode channel B output is delayed an additional 1/2 cycle. Signal S1 (Pin 8) and signal S2 (Pin 9) are both held high. This is set at jumpers E22–E29 and E26–E28.

Data Format Select

Data Format Select sets the output data format that the ADC outputs. Setting DFS (Pin 4) low at E30–E27 sets the output format to be offset binary; setting DFS high at E30–E25 sets the output to be twos complement.

Data Outputs

The ADC digital outputs are latched on the board by two 574s, the latch outputs are available at the 37-pin connector at Pins 22–29 (Channel A) and Pins 30–37 (Channel B). A latch output clock (data ready) is available at Pin 2 or 21 on the output connector. The data ready signal can be aligned with clock A input by connecting E31–E32 or aligned with clock B input by connecting E31–E33.

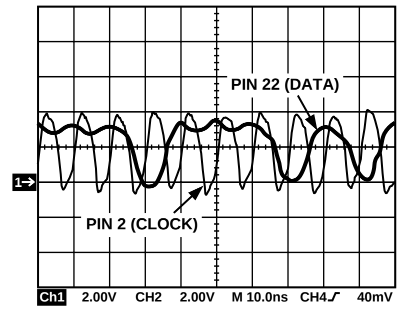


Figure 24. Data Output and Clock at 37-Pin Connector

DAC Outputs

Each channel is reconstructed by an on-board dual channel DAC, an AD9763. This DAC is intended to assist in debug—it should not be used to measure the performance of the ADC. It is a current output DAC with on-board 50 Ω termination resistors. Figure 25 is representative of the DAC output with a full-scale analog input. The scope setting was low bandwidth, 50 Ω termination.

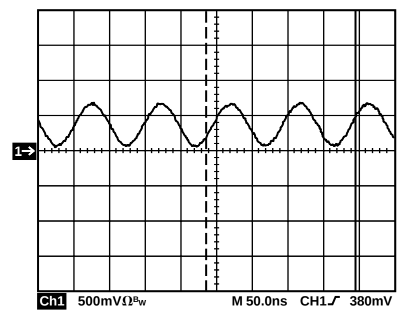


Figure 25. AD9763 Reconstruction DAC Output

Troubleshooting

If the board does not seem to be working correctly, try the following:

- Verify power at IC pins.
- Check that all jumpers are in the correct position for the desired mode of operation.
- Verify VREF is at 1.25 V
- Try running encode clock and analog inputs at low speeds (10 MSPS/1 MHz) and monitor 574 outputs, DAC outputs, and ADC outputs for toggling.

The AD9288 Evaluation Board is provided as a design example for customers of Analog Devices, Inc. ADI makes no warranties, express, statutory, or implied, regarding merchantability or fitness for a particular purpose.

BILL OF MATERIALS

#	QTY	REFDES	DEVICE	PACKAGE	VALUE
1	22	C1–C15, C20–C25, C27	Ceramic Cap	0603	0.1 μF
2	5	C16–C19, C26	Tantalum Cap	TAJD	10 μF
3	43	E1–E43	W-HOLE	W-HOLE	
4	8	J1–J8	SMBPN	SMBP	
5	1	P1	TB6	TB6	
6	1	P2	37DRFP	C37DRFP	
7	10	R1, R3, R5–R7, R10–R14	Resistor	R1206	50 Ω
8	2	R2, R4	Resistor	R1206	25 Ω
9	2	R8, R9	Resistor	R1206	2 kΩ
10	2	R15, R16	Resistor	R1206	0 Ω
11	2	T1, T2	Transformer	T1–1T	
12	1	U1	AD9288	LQFP48	
13	1	U2	AD9763	LQFP48	
14	2	U3, U4	74ACQ574	DIP20\SOL	
15	2	U5, U6	SN74LCX86	SO14	

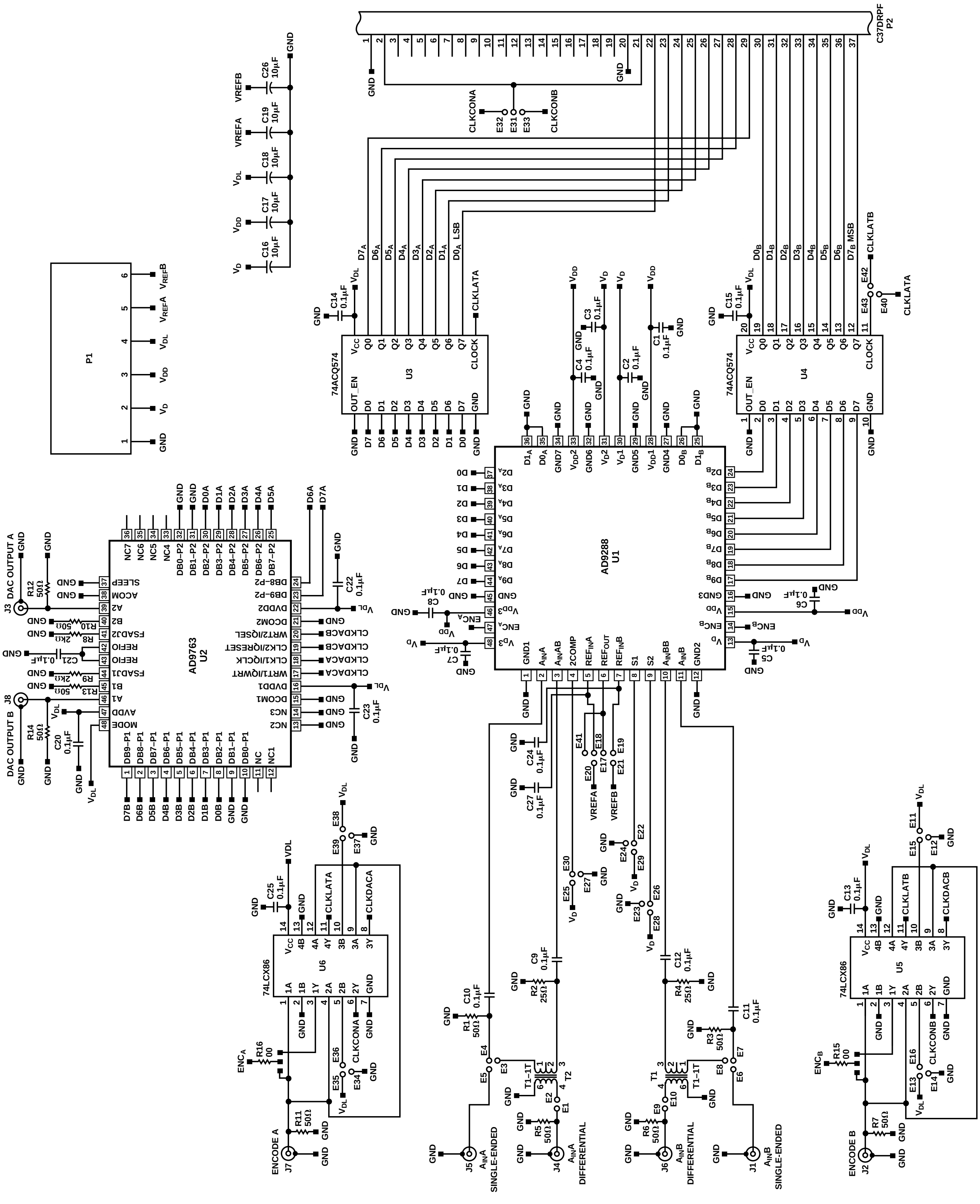


Figure 26 . Dual Evaluation Board Schematic

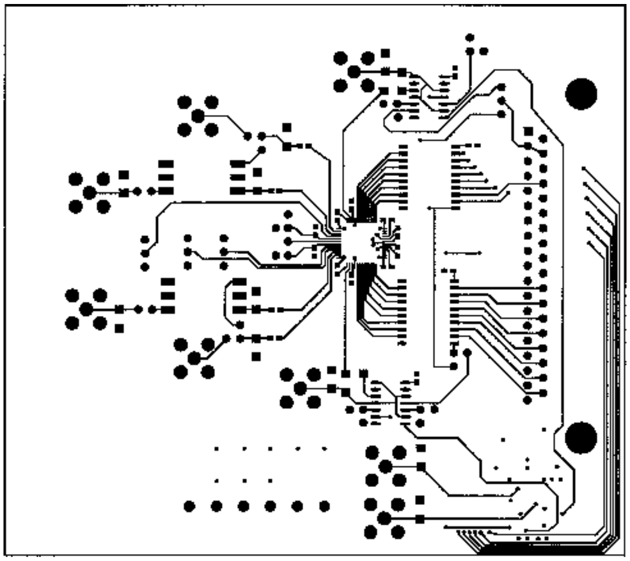


Figure 27. Printed Circuit Board Top Side Copper

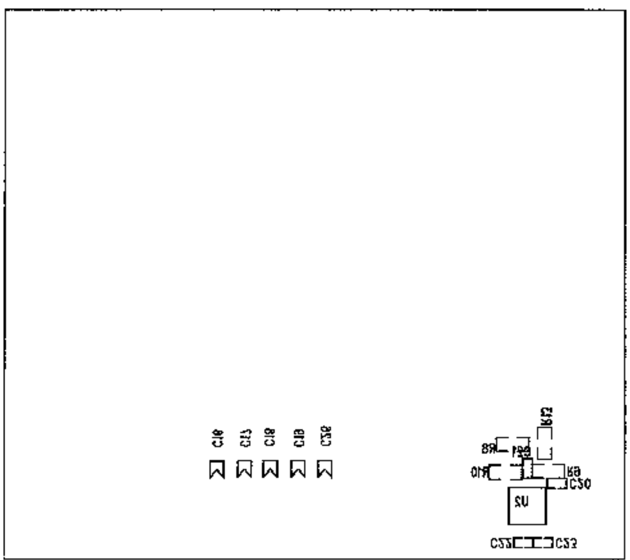


Figure 28. Printed Circuit Board Bottom Side Silkscreen

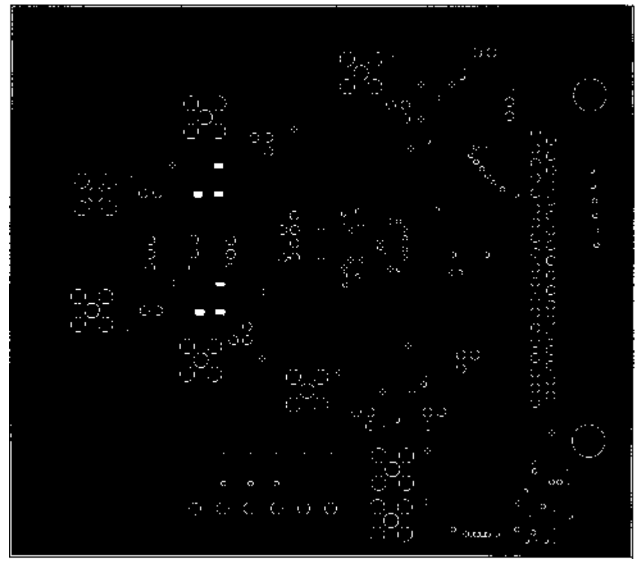


Figure 29. Printed Circuit Board Ground Layer

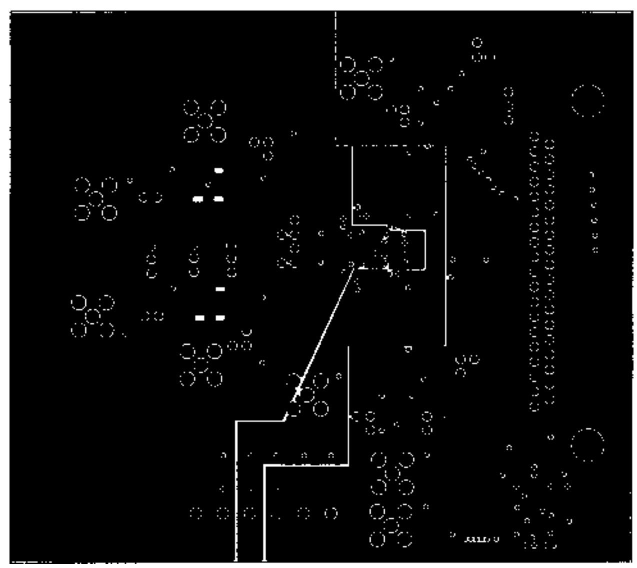


Figure 30. Printed Circuit Board "Split" Power Layer

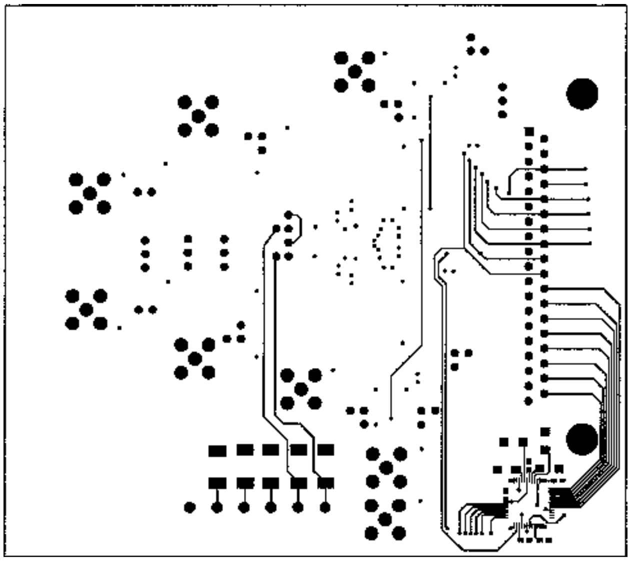


Figure 31. Printed Circuit Board Bottom Side Copper

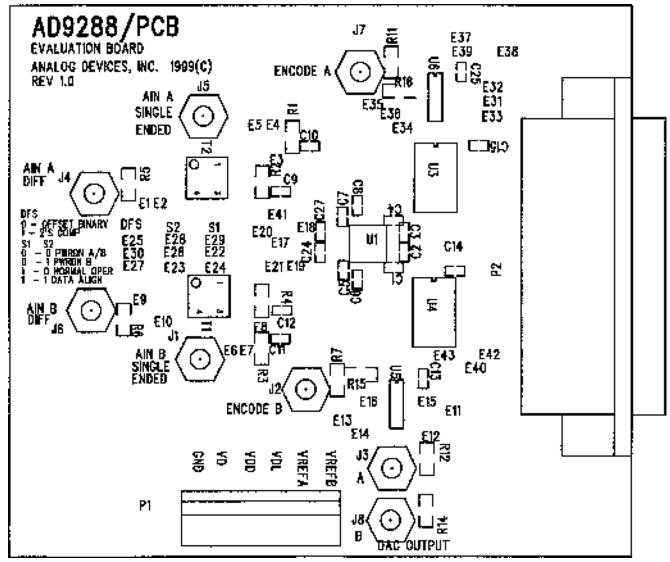
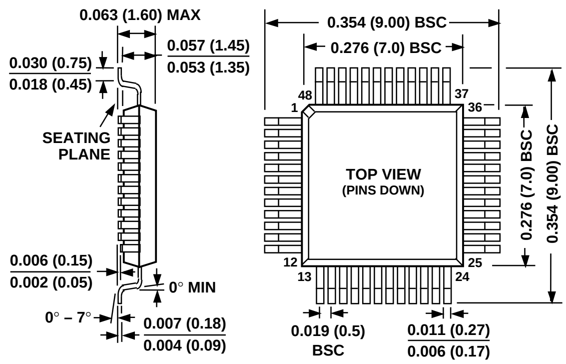


Figure 32. Printed Circuit Board Top Side Silkscreen

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

48-Lead LQFP
(ST-48)



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