10-Bit, 12-Channel Output Decimating LCD Driver

AD8386

FEATURES

- **High voltage drive**
  - **To within 1.3 V of supply rails**
- **Output short-circuit protection**
- **High update rates**
  - **Fast, 100 Ms/s 10-bit input data update rate**
- **Static power dissipation: 1.4 W**
- **Voltage-controlled video reference (brightness), offset, and full-scale (contrast) output levels**
- **INV bit reverses polarity of video signal**
- **3.3 V logic, 9 V to 18 V analog supplies**
- **High accuracy voltage outputs**
  - **Laser trimming eliminates the need for adjustments or calibration**
- **Flexible logic**
  - **XFR allows parallel AD8386 operation**
- **Fast settling into capacitive loads**
  - **35 ns settling time to 0.25% into 150 pF load**
  - **Slew rate 400 V/µs**
- **Available in 64-lead 9 mm × 9 mm LFCSP_VQ**

GENERAL DESCRIPTION

The AD8386 provides a fast, 10-bit, latched, decimating digital input that drives 12 high voltage outputs. Input words with 10 bits are loaded sequentially into 12 separate high speed, bipolar DACs. Flexible digital input format allows several AD8386s to be used in parallel in high resolution displays. The output signal can be adjusted for dc reference, signal inversion, and contrast for maximum flexibility.

The AD8386 is fabricated on ADI's fast bipolar, 26 V XFHV process, which provides fast input logic, bipolar DACs with trimmed accuracy and fast settling, high voltage, precision drive amplifiers on the same chip.

The AD8386 dissipates 1.4 W nominal static power.

The AD8386 is offered in a 64-lead 9 mm × 9 mm LFCSP_VQ package and operates over the commercial temperature range of 0°C to 85°C.

FUNCTIONAL BLOCK DIAGRAM

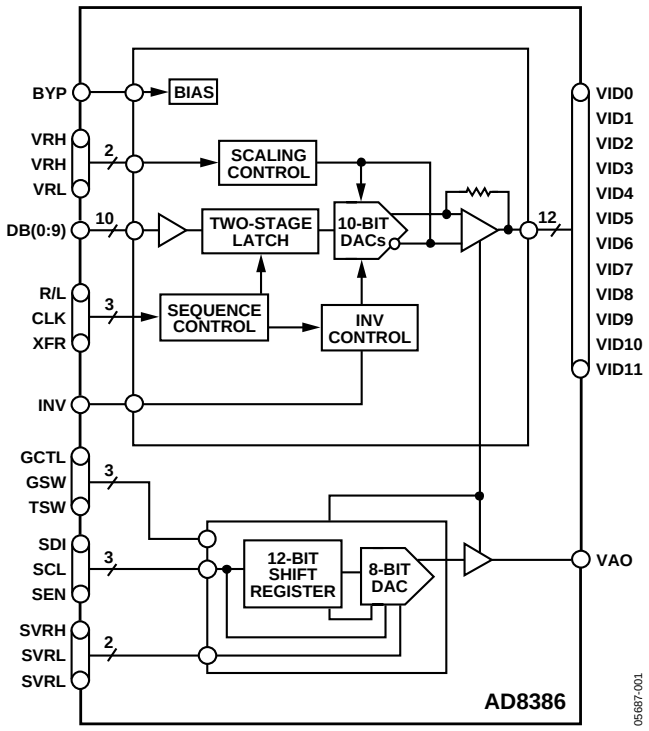

Figure 1.

Rev. 0

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TABLE OF CONTENTS

REVISION HISTORY

8/05—Revision 0: Initial Version

SPECIFICATIONS

DECDRIVER® SECTION

At 25°C, AVCC = 15.5 V, DVCC = 3.3 V, $T_{A\ MIN}$ = 0°C, $T_{A\ MAX}$ = 85°C, VRH = 9.5 V, VRL = 7 V, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
VIDEO DC PERFORMANCE[1]	$T_{A\ MIN}$ to $T_{A\ MAX}$				
VDE	DAC Code 450 to 800	−7.5		+7.5	mV
VCME	DAC Code 450 to 800	−3.5		+3.5	mV
VIDEO OUTPUT DYNAMIC PERFORMANCE	$T_{A\ MIN}$ to $T_{A\ MAX}$, C_L = 150 pF				
Data Switching Slew Rate	20% to 80%, V_O = 5 V step		400		V/µs
Invert Switching Slew Rate	20% to 80%, V_O = 10 V step		560		V/µs
Data Switching Settling Time to 1%			24	35	ns
Data Switching Settling Time to 0.25%			35	50	ns
Invert Switching Settling Time to 1%			80	130	ns
Invert Switching Settling Time to 0.25%			250	500	ns
Invert Switching Overshoot	10 V Step		100	200	mV
CLK and Data Feedthrough[2]			15		mV p-p
All-Hostile Crosstalk[3]					
Amplitude			50		mV p-p
Glitch Duration			30		ns
DAC Transition Glitch Energy	DAC code 511 to 512		0.6		nV-s
VIDEO OUTPUT CHARACTERISTICS					
Output Voltage Swing	AVCC – VOH, VOL – AGND		1.1	1.3	V
Output Voltage—Grounded Mode			200		mV
Data Switching Delay: t_9[4]	5 V step	12	14	16	ns
INV Switching Delay: t_{10}[5]	10 V step	15	17	19	ns
Output Current			100		mA
Output Resistance			29		Ω
REFERENCE INPUTS					
VRL Range	VRH ≥ VRL	5.25		AVCC – 4	V
VRH Range	VRH ≥ VRL	VRL		AVCC	V
VRH – VRL Range	VFS = 2 × (VRH – VRL)	0		2.75	V
VRH Input Resistance	To VRL		20		kΩ
VRL Input Current			−45		µA
VRH Input Current			125		µA
RESOLUTION					
Coding	Binary	10			Bits
DIGITAL INPUT CHARACTERISTICS					
C_{IN}				3	pF
I_{IH}			0.05		µA
I_{IL}			−2		µA
V_{IH}		2			V
V_{IL}				0.8	V
V_{TH}			1.65		V
I_{IH} TSW			330		µA
I_{IL} TSW			−2		µA
TSW $R_{PULLDOWN}$			10		kΩ

Parameter	Conditions	Min	Typ	Max	Unit
DIGITAL TIMING CHARACTERISTICS	$T_{A\ MIN}$ to $T_{A\ MAX}$				
Maximum Input Data Update Rate		100			Ms/s
Data Setup Time: t_1		1			ns
XFR Setup Time: t_3		0			ns
INV Setup Time: t_{11}		0			ns
Data Hold Time: t_2		3.5			ns
XFR Hold Time: t_4		4.5			ns
INV Hold Time: t_{12}		4			ns
CLK High Time: t_7		6			ns
CLK Low Time: t_8		4			ns

[1] VDE = differential error voltage. VCME = common-mode error voltage. Full-scale output voltage = VFS = 2 × (VRH − VRL). See the Accuracy section.
[2] Measured on two outputs differentially as CLK and DB (0:9) are driven and XFR is held low.
[3] Measured on two outputs differentially as the others are transitioning by 5 V. Measured for both states of INV.
[4] Measured from 50% of rising CLK edge to 50% of output change. Measurement is made for both states of INV.
[5] Measured from 50% of rising CLK edge, which follows a valid XFR, to 50% of output change. See Figure 6 for the definition.

SERIAL INTERFACE SECTION

At 25°C, AVCC = 15.5 V, DVCC = 3.3 V, $T_{A\ MIN}$ = 0°C, $T_{A\ MAX}$ = 85°C, VRH = 9.5 V, VRL = 7 V, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
SERIAL DAC DC PERFORMANCE					
DNL	SVFS = 5 V	−1		+1	LSB
INL	SVFS = 5 V	−1.5		+1.5	LSB
Output Offset Error		−2.0		+2.0	LSB
Scale Factor Error		−3.0		+3.0	LSB
SERIAL DAC OUTPUT DYNAMIC PERFORMANCE	To 0.5%				
VAO Settling Time, t_{26}	C_L = 100 pF		1	2	µs
VAO Settling Time, t_{26}	C_L = 33 µF			15	ms
SERIAL DAC OUTPUT CHARACTERISTICS					
VAO Maximum			SVRH − 1 LSB		V
VAO Minimum			SVRL		V
VAO − Grounded Mode			150		mV
VAO Output Resistance	All supplies OFF		75		kΩ
I_{OUT}			±30		mA
C_{LOAD} Low Range[1]				0.002	µF
C_{LOAD} High Range[1]		0.047			µF
REFERENCE INPUTS					
SVRH Range	SVRL < SVRH	SVRL + 1		AVCC − 3.5	V
SVRL Range	SVRL < SVRH	AGND + 1.5		SVRH − 1	V
SVFS Range		1		8	V
SVRH Input Current	SVRS = 5 V		0.1		µA
SVRL Input Current	SVRS = 5 V	−1.6	−1.3		mA
DIGITAL INPUT CHARACTERISTICS					
C_{IN}				3	pF
I_{IH}			0.05		µA
I_{IL}			−1		µA
V_{IH}		2.0		DVCC	V
V_{IL}		DGND		0.8	V
V_{TH}			1.65		V
DIGITAL TIMING CHARACTERISTICS	$T_{A\ MIN}$ to $T_{A\ MAX}$				
SEN to SCL Setup Time, t_{20}		10			ns
SCL, High Level Pulse Width, t_{21}		10			ns
SCL, Low Level Pulse Width, t_{22}		10			ns
SCL to SEN Hold Time, t_{23}		10			ns
SDI Setup Time, t_{24}		10			ns
SDI Hold Time, t_{25}		10			ns
POWER SUPPLIES					
DVCC, Operating Range		3	3.3	3.6	V
DVCC, Quiescent Current			54	75	mA
AVCC Operating Range		9		18	V
Total AVCC Quiescent Current			80	100	mA
OPERATING TEMPERATURES					
Ambient Temperature Range, T_A[2]	Still air, TSW = HIGH	0		70	°C
Ambient Temperature Range, T_A[2]	Still air, TSW = LOW	0		85	°C

[1] Output VAO is designed to drive capacitive loads less than 0.002 µF or more than 0.047 µF. Load capacitances in the range 0.002 µF − 0.047 µF cause the output overshoot to exceed 100 mV.

[2] Operation at high ambient temperature requires a thermally optimized PCB layout (see the Applications section). In systems with limited or no airflow, the maximum ambient operating temperature is limited to 70°C with the thermal protection enabled, VFS = 4 V, data update rate = 85 Ms/s. Operation at 85°C ambient temperature requires the thermal protection circuit turned disabled (TSW = LOW).

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	
AVCCx – AGNDx	18 V
DVCC – DGND	4.5 V
Input Voltage	
Maximum Digital Input Voltage	DVCC + 0.5 V
Minimum Digital Input Voltage	DGND – 0.5 V
Maximum Analog Input Voltage	AVCC + 0.5 V
Minimum Analog Input Voltage	AGND – 0.5 V
Internal Power Dissipation[1]	
LFCSP @ T_A = 25°C	3.7 W
Operating Temperature Range	0°C to 85°C
Storage Temperature Range	–65°C to +125°C
Lead Temperature Range (Soldering 10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[1] 64-lead VQ_LFCSP:
θ_{JA} = 27°C/W in still air (JEDEC STD, 4-layer PCB with 16 vias on Epad)
θ_{JA} = 25°C/W @ 200 lfm airflow (JEDEC STD, 4-layer PCB with 16 vias on Epad)
θ_{JA} = 24°C/W @ 400 lfm airflow (JEDEC STD, 4-layer PCB with 16 vias on Epad)
Ψ_{JT} = 0.2°C/W in still air (JEDEC STD, 4-layer PCB with 16 vias on Epad)
Ψ_{JB} = 13.8°C/W in still air (JEDEC STD, 4-layer PCB with 16 vias on Epad)

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8386 is limited by its junction temperature. The maximum safe junction temperature for plastic encapsulated devices, as determined by the glass transition temperature of the plastic, is approximately 150°C. Exceeding this limit temporarily may cause a shift in the parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

OVERLOAD PROTECTION

The AD8386 overload protection circuit consists of an output current limiter and a thermal protection circuit.

When TSW is LOW, the thermal protection circuit is disabled, and the output current limiter is turned on. The maximum current at any one output of the AD8386 is internally limited to 100 mA average. In the event of a momentary short circuit between a video output and a power supply rail (AVCC or AGND), the output current limit is sufficiently low to provide temporary protection.

When TSW is HIGH, the output current limiter, as well as the thermal protection circuit, is turned on. The thermal protection circuit debiases the output amplifier when the junction temperature reaches the internally set trip point. In the event of an extended short circuit between a video output and a power supply rail, the output amplifier current continues to switch between 0 mA and 100 mA typical with a period determined by the thermal time constant and the hysteresis of the thermal trip point. The thermal protection circuit limits the average junction temperature to a safe level, which provides long-term protection.

EXPOSED PADDLE

To ensure optimal thermal performance, the exposed paddle must be electrically connected to an external plane, such as AVCC or GND, as described in the Applications section.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

OPERATING TEMPERATURE RANGE

The maximum operating junction temperature is 150°C. The junction temperature trip point of the thermal protection circuit is 165°C. Production tests guarantee a minimum junction temperature trip point of 125°C.

Consequently, the maximum guaranteed operating junction temperature is 125°C when the thermal protection circuit is enabled and 150°C when the thermal protection circuit is disabled.

To ensure operation within the specified operating temperature range, it is necessary to limit the maximum power dissipation as

$$P_{DMAX} \approx \frac{(T_{JMAX} - T_A)}{\theta_{JA\ Still\ Air} - 0.09 \times (Airflow\ in\ lfm)^{0.59}}$$

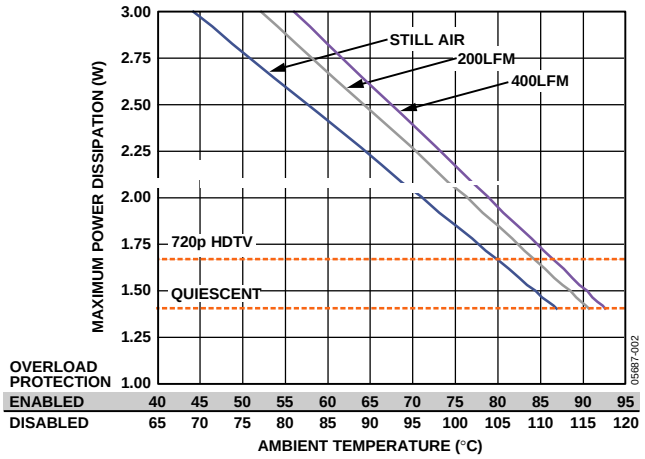


Figure 2. Maximum Power Dissipation vs. Temperature

The AD8386 is on a 4-layer JEDEC PCB with a thermally optimized landing pattern with 16 vias.

The quiescent power dissipation of the AD8386 is 1.4 W.

When driving a 12-channel 720p HDTV panel with an input capacitance of 150 pF, the AD8386 dissipates 1.66 W when displaying 1 pixel wide alternating white and black vertical lines generated by a standard 720p HDTV input video.

Conditions include the following:

- AVCC = 15.5 V
- DVCC = 3.3 V
- VFS = 5 V
- C_L = 150 pF
- f_{PIXEL} = 74.25 MHz
- Black-to-white transition = 4 V
- Active video time = 75%

Figure 2 shows these power dissipations.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

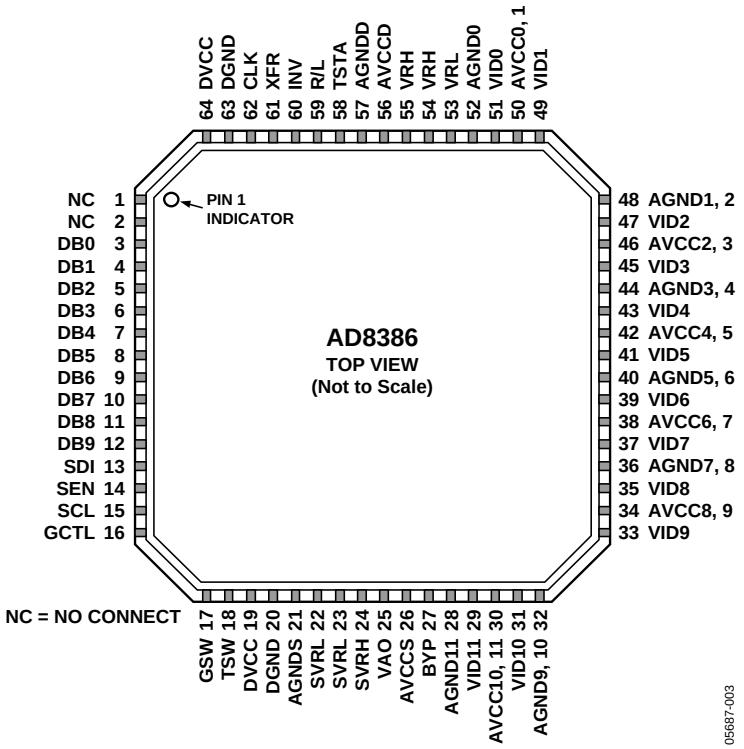


Figure 3. 64-Lead LFCSP_VQ Pin Configuration

Table 4. 64-Lead LFCSP_VQ Pin Function Descriptions

Pin No.	Mnemonic	Function	Description
1, 2	NC	No Connect	No Internal Connection.
3 to 12	DB0 to DB9	Data Input	10-Bit Data Input. MSB = DB(9).
13	SDI	Serial Data Input	While the SEN input is LOW, one 12-bit serial word is loaded into the serial DAC on the rising edges of the SCL.
14	SEN	Serial DAC Enable	A falling edge of this input initiates a loading cycle. While this input is held LOW, the serial DAC is enabled and data is loaded on every rising edge of SCL. The output is updated on the rising edge of a valid SEN. A valid SEN must remain LOW for at least three SCL cycles. While this input is held HIGH, the control DAC is disabled.
15	SCL	Serial Data Clock	Serial Data Clock.
16	GCTL	Output Mode Control	When this input is HIGH, the output mode is determined by the function programmed into the serial interface. When LOW, the output mode is controlled by the GSW input.
17	GSW	Output Mode Switch	When GCTL is LOW and this input is HIGH, the video outputs and VAO operate normally. When GCTL and this input are both LOW, the video outputs and VAO are asynchronously forced to AGND, regardless of the function programmed into the serial interface. This function operates when AVCC power is OFF but requires DVCC power supply to be ON.
18	TSW	Thermal Switch	When this input is LOW, the thermal protection circuit is disabled. When HIGH, the thermal protection circuit is enabled. This pin has a 10 kΩ internal pull-down resistor.
19, 64	DVCC	Digital Power Supply	Digital Power Supply.
20, 63	DGND	Digital Ground	Digital Supply Return.
21	AGNDS	Analog Ground	Analog Supply Return.
22, 23, 24	SVRL, SVRH	Serial DAC Reference Voltage	The voltage applied between these pins sets the serial DAC full-scale voltage.
25	VAO	Serial DAC Output	This output voltage is updated in the rising edge of the SEN input.
26	AVCCS	Analog Power Supply	Analog Power Supply.
27	BYP	Bypass	A 0.1 µF capacitor connected between this pin and AGND ensures optimum settling time.
28, 32, 36, 40, 44, 48, 52	AGND11 to AGND0	Analog Ground	Analog Supply Returns.
29, 31, 33, 35, 37, 39, 41, 43, 45, 47, 49, 51	VID11 to VID0	Analog Output	These pins are directly connected to the analog inputs of the LCD panel.
30, 34, 38, 42, 46, 50	AVCC10, 11 to AVCC0, 1	Analog Power Supply	Analog Power Supplies.
53	VRL	Video Center Reference	The voltage applied to this pin sets the video center voltage. The video outputs are above this reference while the INV = HIGH and below this reference while INV = LOW.
54, 55	VRH	Full-Scale Reference	The full-scale video output voltage is VFS = 2 × (VRH − VRL).
56	AVCCD	Analog Power Supply	Analog Power Supply.
57	AGNDD	Analog Ground	Analog Supply Return.
58	TSTA	Test Pin	Connect this pin to AGND.
59	R/L	Right/Left Select	A new data loading sequence begins on the left with Channel 0 when this input is LOW, and on the right with Channel 11 when this input is HIGH.
60	INV	Invert	When this input is HIGH, the VIDx output voltages are above VRL. When LOW, the VIDx outputs voltages are below VRL. The state of INV is latched on the first rising CLK edge after XFR is detected. The VIDx outputs change on the rising CLK edge after the next XFR is detected.
61	XFR	Transfer/Start Sequence	The state of XFR is detected on the rising edge of CLK. Data is transferred to the outputs and a new loading sequence begins on the next rising edge of CLK after XFR is detected HIGH.
62	CLK	Clock	Video Data Clock.

DECDRIVER BLOCK DIAGRAM AND TIMING

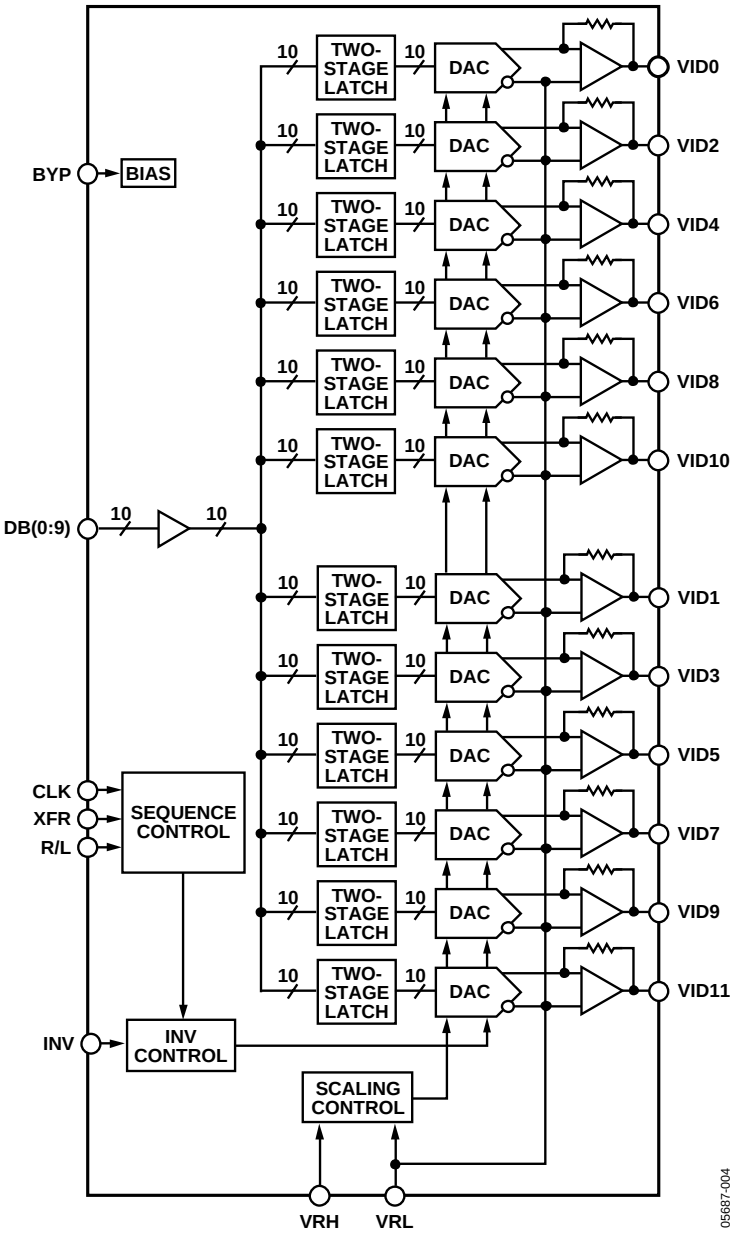


Figure 4. AD8386 DecDriver Section

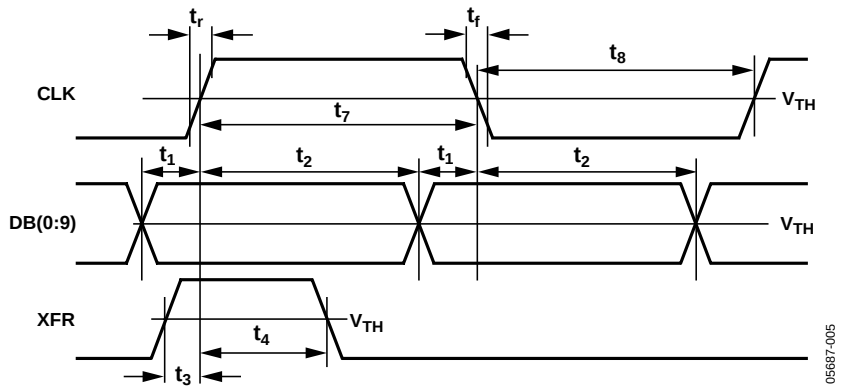


Figure 5. Input Timing

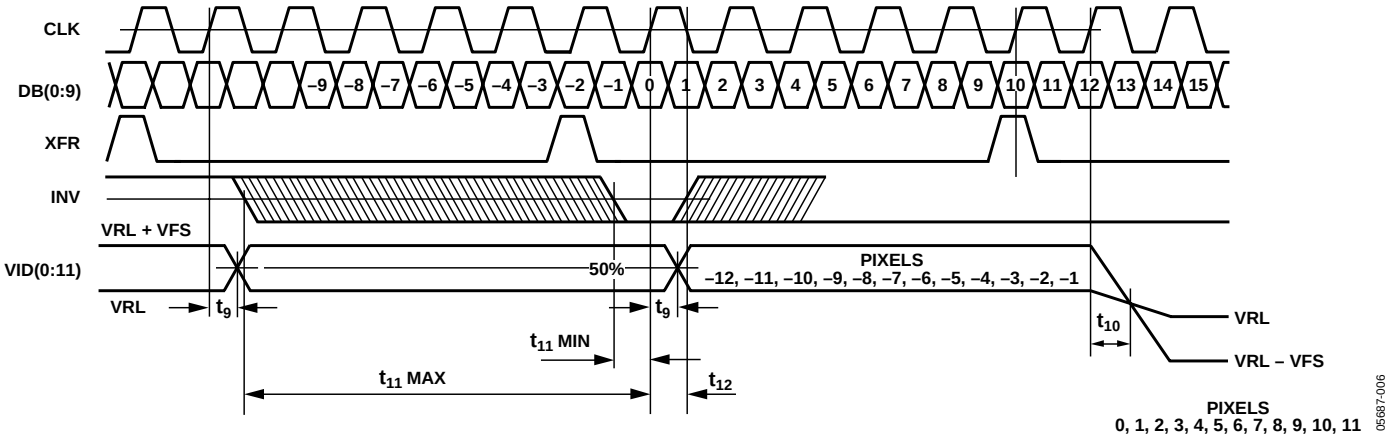


Figure 6. Output Timing (R/L LOW)

Table 5.

Parameter	Conditions	Min	Typ	Max	Unit
Data Setup Time, t_1	Input t_r, t_f = 2 ns	1			ns
Data Hold Time, t_2		3.5			ns
XFR Setup Time, t_3		0			ns
XFR Hold Time, t_4		4.5			ns
CLK High Time, t_7		6			ns
CLK Low Time, t_8		4			ns
Data Switching Delay, t_9		12	14	16	ns
Invert Switching Delay, t_{10}		15	17	19	ns
Invert Setup Time, t_{11}		0			ns
Invert Hold Time, t_{12}		4			ns

SERIAL INTERFACE BLOCK DIAGRAM AND TIMING

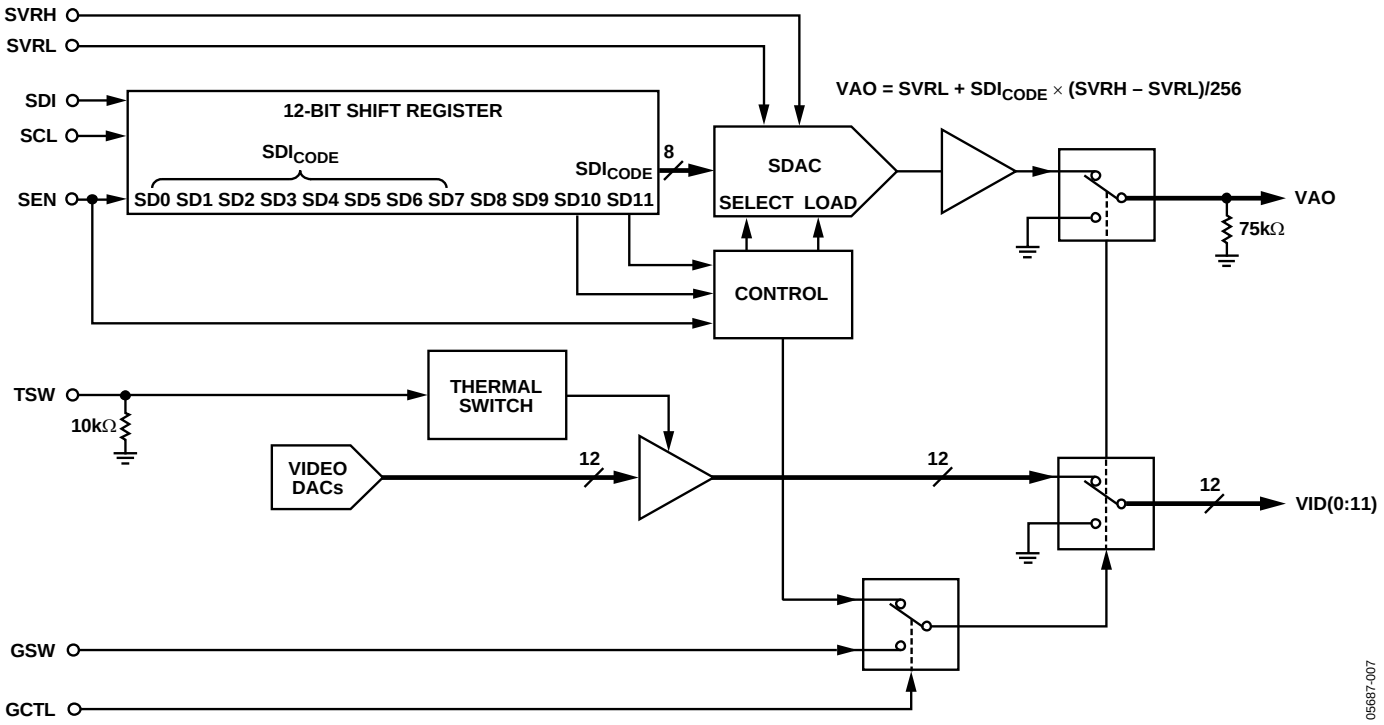


Figure 7. Serial Interface Block Diagram

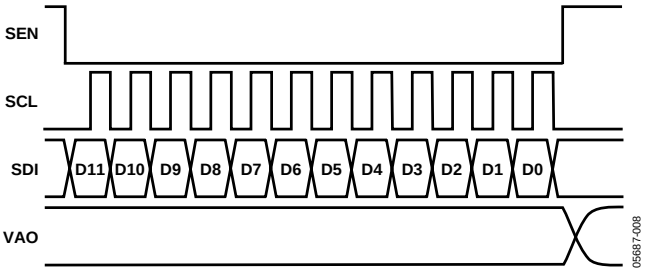


Figure 8. Serial Interface Timing Diagram

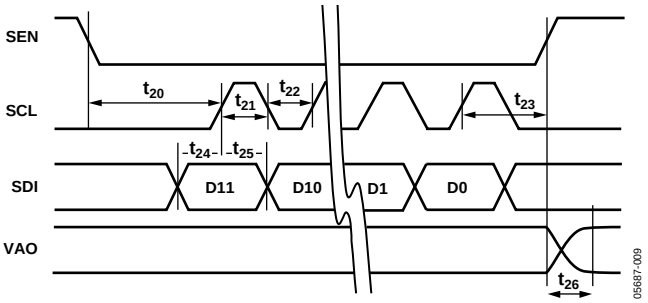


Figure 9. Serial Interface Timing Diagram

Table 6.

Parameter	Conditions	Min	Typ	Max	Unit
SEN to SCL Setup Time, t_{20}		10			ns
SCL, High Level Pulse Width, t_{21}		10			ns
SCL, Low Level Pulse Width, t_{22}		10			ns
SCL to SEN Hold Time, t_{23}		10			ns
SDI Setup Time, t_{24}		10			ns
SDI Hold Time, t_{25}		10			ns
VAO Settling Time, t_{26}	SVFS = 5 V, to 0.5 %, C_L = 100 pF		1	2	µs
VAO Settling Time, t_{26}	SVFS = 5 V, to 0.5 %, C_L = 33 µF			15	ms

FUNCTIONAL DESCRIPTION

The AD8386 is a system building block designed to directly drive the columns of LCD microdisplays of the type popularized for use in projection systems. It has 12 channels of precision, 10-bit digital-to-analog converters (DACs) loaded from a single high speed serial input. Precision current feedback amplifiers, which provide well-damped pulse response and fast voltage settling into large capacitive loads, buffer the 12 outputs. Laser trimming at the wafer level ensures low absolute output errors and tight channel-to-channel matching. Tight part-to-part matching in high resolution systems is guaranteed by the use of external voltage references.

REFERENCE AND CONTROL INPUT DESCRIPTIONS

Data transfer/start sequence control—input data loading, data transfer.

A valid XFR control input initiates a new six-clock loading cycle, during which data is transferred to the outputs, and 12 input data-words are loaded sequentially into the 12 internal channels. Data is loaded on both the rising and falling edges of CLK. Data loaded from the previous cycle is transferred to the outputs on the rising CLK edge when the XFR is held HIGH at the preceding rising CLK edge only. A new loading sequence begins on the current rising CLK edge when XFR is held HIGH at the preceding rising CLK edge only.

Right/left control—input data loading.

To facilitate image mirroring, the direction of the loading sequence is set by the R/L control.

A new loading sequence begins at Channel 0 and proceeds to Channel 11 when the R/L control is held LOW. It begins at Channel 11 and proceeds to Channel 0 when the R/L control is held HIGH.

VRH, VRL inputs—full-scale video reference inputs.

The full-scale output voltage is VFS = 2 × (VRH − VRL).

INV control—analog output inversion.

The analog voltage equivalent of the input code is subtracted from (VRL + VFS) while INV is held HIGH, and added to (VRL − VFS) while INV is held LOW.

The state of the INV input is latched on the first rising edge of CLK, immediately following a valid XFR. The VIDx outputs invert on the first rising CLK edge, immediately following the next valid XFR.

TSW control—thermal switch control.

When this input is HIGH, the thermal protection circuit is enabled. When LOW or left unconnected, the thermal protection circuit is disabled.

An internal 10 kΩ pull-down resistor disables the thermal switch when this pin is left unconnected.

GCTL, GSW controls—output mode control.

Table 7. GTCL, GSW Truth Table

GTCL	GSW	Action
0	0	All video outputs and VAO are forced near AGND. While the outputs are disabled, AVCC can be removed.
0	1	All video outputs and VAO operate normally.
1	X	Output operating mode is controlled by the serial interface.

TRANSFER FUNCTION AND ANALOG OUTPUT VOLTAGE

The *DecDriver* has two regions of operation where the video output voltages are either above or below the reference voltage VRL. The transfer function defines the video output voltage as the function of the digital input code as

$$VIDx(n) = VRL + VFS \times (1 - n/1023), \text{ for INV = HIGH}$$

$$VIDx(n) = VRL - VFS \times (1 - n/1023), \text{ for INV = LOW}$$

where:

n = input code

$VFS = 2 \times (VRH - VRL)$

A number of internal limits define the usable range of the video output voltages, VIDx, shown in Figure 10.

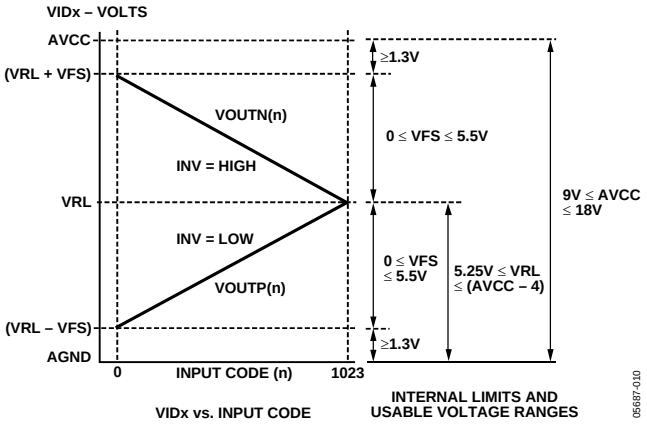


Figure 10. Transfer Function and Usable Voltage Ranges

ACCURACY

To best correlate transfer function errors to image artifacts, the overall accuracy of the *DecDriver* is defined by two parameters, VDE and VCME.

VDE, the differential error voltage, measures the difference between the rms value of the output and the rms value of the ideal. The defining expression is

$$VDE(n) = \frac{[VOUTN(n) - VOUTP(n)]}{2} - \left(1 - \frac{n}{1023}\right) \times VFS$$

VCME, the common-mode error voltage, measures ½ the dc offset of the output. The defining expression is

$$VCME(n) = \frac{1}{2}\left[\frac{VOUTN(n) + VOUTP(n)}{2} - VRL\right]$$

3-WIRE SERIAL INTERFACE

The serial interface controls the 8-bit serial DAC and the video output operating mode via a 12-bit serial word. The two most significant bits (MSB) select the function and the eight least significant bits (LSB) are the data for the serial DAC.

Table 8. Bit Definitions

Bit Name	Bit Functionality
SD (0:7)	8-Bit SDAC Data. MSB = SD7.
SD8	Not Used.
SD9	Not Used.
SD10	VAO Load Selection.
SD11	Output Mode Selection When GCTL = 1.

Table 9. Truth Table @ GCTL = HIGH

SEN	SD				Action
	11	10	9	8	
↑	0	0	X	X	Normal Output Mode. No change to VAO.
↑	0	1	X	X	Normal Output Mode. Load VAO.
↑	1	0	X	X	Grounded Output Mode. No change to VAO.
↑	1	1	X	X	Grounded Output Mode. Load VAO.
↓	X	X	X	X	Start a Serial Interface Loading Cycle. No change to VAO.

Table 10. Truth Table @ GCTL = LOW

SEN	SD				Action
	11	10	9	8	
↑	X	0	X	X	No Change to VAO.
↑	X	1	X	X	Load VAO.
↓	X	X	X	X	Start a Serial Interface Loading Cycle. No change to VAO.

Serial DAC

The serial DAC is loaded via the serial interface. The output voltage is determined by

$$VAO = SVRL + (SVRH - SVRL) \times n/256$$

where n is the $SD(0:7)$ serial input code.

Output VAO is designed to drive capacitive loads less than 0.002 µF or more than 0.047 µF. Load capacitances in the 0.002 µF – 0.047 µF range cause the output overshoot to exceed 100 mV.

OUTPUT OPERATING MODES

In normal operating mode, the voltage of the video outputs is determined by the inputs.

In grounded output mode, the video outputs are forced to (AGND + 0.2 V) typ.

OVERLOAD PROTECTION

The overload protection employs current limiters and a thermal protection circuit to protect the video output pins against accidental shorts between any video output pin and AVCC or AGND.

The junction temperature trip point of the thermal protection circuit is 165°C. Production tests guarantee a minimum junction temperature trip point of 125°C. Consequently, the operating junction temperature should not rise above 125°C when the thermal protection circuit is enabled.

For systems that operate at high internal ambient temperatures and require large capacitive loads to be driven by the AD8386 at high frequencies, junction temperatures above 125°C may be required. In such systems, the thermal protection circuit should either be disabled or a minimum airflow of 200 lfm must be maintained.

APPLICATIONS

OPTIMIZED RELIABILITY WITH THE THERMAL PROTECTION CIRCUIT

The AD8386 is designed for enhanced reliability through features that provide protection against accidental shorts that may occur during PCB assembly repair, such as solder bridging, or during system assembly, such as a misaligned flat panel cable in the connector.

While internal current limiters provide short-term protection against temporary shorts at the outputs, the thermal shutdown provides protection against persistent shorts lasting for several seconds. To optimize reliability, the following sequence of operations is recommended.

Initial Power-Up after PCB Assembly or Repair

Disable grounded output mode and enable thermal protection.

Ensure that the GCTL and GSW pins are LOW and the TSW pin is HIGH upon initial power-up and remains unchanged throughout this procedure.

- Execute the initial power-up.
- Identify any shorts at the outputs.
- Power-down, repair shorts, and repeat the initial power-up sequence until proper system functionality is verified.

Power-Up during Normal Operation

Disable grounded output mode and disable the thermal protection circuit using either of the following two methods:

- GCTL = HIGH, TSW = HIGH and serial code 0XXXXXXXXXXX sent immediately following a power-up, places all outputs into normal operating mode and disables the thermal protection circuit.
- TSW = LOW disables the thermal protection circuit. GCTL = LOW and GSW = HIGH puts all outputs into normal operating mode.

OPERATION IN HIGH AMBIENT TEMPERATURE

To extend the maximum operating junction temperature of the AD8386 to 150°C, keep the thermal protection circuit disabled (TSW = LOW) during normal operation.

POWER SUPPLY SEQUENCING

As indicated in the Absolute Maximum Ratings section, the voltage at any input pin cannot exceed its supply voltage by more than 0.5 V. Power-on and power-off sequencing may be required to comply with the Absolute Maximum Ratings.

Failure to comply with the Absolute Maximum Ratings may result in functional failure or damage to the internal ESD diodes. Damaged ESD diodes may cause temporary parametric failures, which may result in image artifacts. Damaged ESD diodes cannot provide full ESD protection, reducing reliability.

The following power supply sequencing ensures that the Absolute Maximum Ratings are not violated.

Power-on sequence is:

- Turn ON AVCC and analog reference voltages.
- Turn ON DVCC and digital signals.

Power-off sequence is:

- Turn OFF AVCC and analog reference voltages.
- Turn OFF DVCC and digital signals.

GROUNDED OUTPUT MODE DURING POWER-OFF

Certain applications require that the video outputs be held near AGND during power-down. The following power-off sequence ensures that the outputs are near ground during power-off and the Absolute Maximum Ratings are not violated.

- Enable grounded output mode in one of two ways: GTCL = LOW and GSW = LOW, or GCTL = HIGH and code 1XXXXXXXXXXX sent via the serial interface.
- Turn OFF AVCC and analog reference voltages.
- Turn OFF DVCC and digital signals.

TYPICAL APPLICATION CIRCUITS

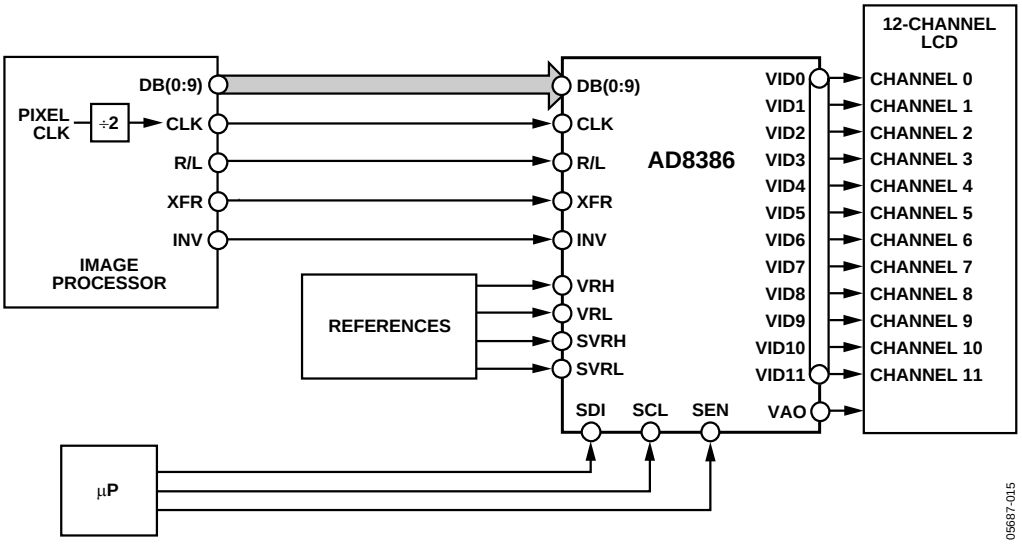


Figure 11. 12-Channel System

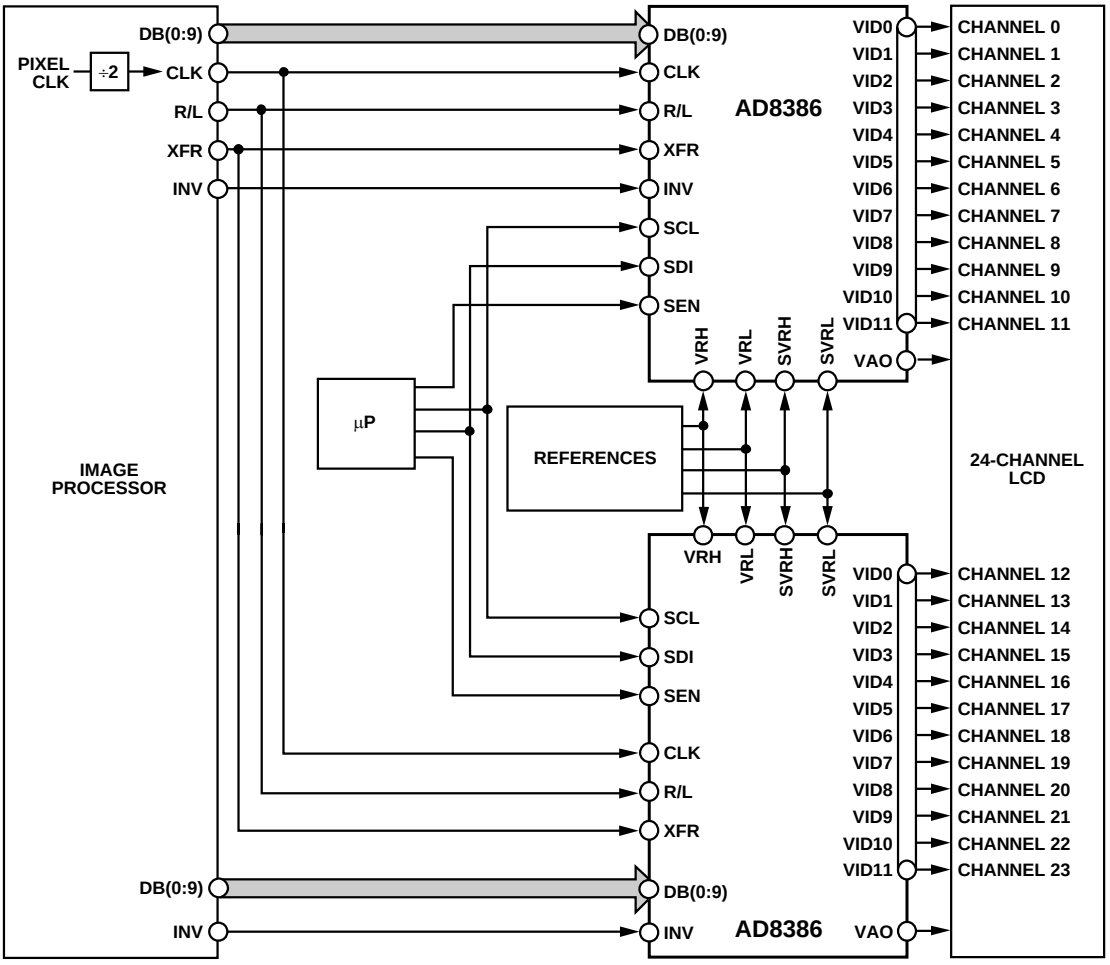


Figure 12. 24-Channel System

PCB DESIGN FOR OPTIMIZED THERMAL PERFORMANCE

The total maximum power dissipated by the AD8386 is partly load dependent. In a 12-channel, 60 Hz XGA system running at a 65 MHz pixel rate, the total maximum power dissipated is 1.7 W, assuming a 15.5 V analog power supply, a 4 V white-to-black swing, and a 150 pF LCD input capacitance.

To limit the operating junction temperature at or below the guaranteed maximum, the package in conjunction with the PCB must effectively conduct heat away from the junction.

The AD8386 package is designed to provide enhanced thermal characteristics through the exposed die paddle on the bottom surface of the package. In order to take full advantage of this feature, the exposed paddle must be in direct thermal contact with the PCB, which then serves as a heat sink.

A thermally effective PCB must incorporate two thermal pads and a thermal via structure. The thermal pad on the top PCB layer provides a solderable contact surface on the top surface of the PCB. The thermal pad on the bottom PCB layer provides a surface in direct contact with the ambient air. The thermal via structure provides a thermal path to the inner and bottom layers of the PCB to remove heat.

Thermal Pad Design

To minimize thermal performance degradation of production PCBs, the contact area between the thermal pad and the PCB should be maximized. Therefore, the size of the thermal pad on the top PCB layer should match the exposed paddle size. The second thermal pad of at least the same size should be placed on the bottom side of the PCB. At least one thermal pad should be in direct thermal contact with a plane, such as AVCC or GND.

Thermal via Structure Design

Effective heat transfer from the top to the inner and bottom layers of the PCB requires thermal vias incorporated into the thermal pad design. Thermal performance increases logarithmically with the number of vias.

Near optimum thermal performance of production PCBs is attained when tightly spaced thermal vias are placed on the full extent of the thermal pad only.

AD8386 PCB DESIGN RECOMMENDATIONS

Table 11. Top PCB Layer

Pad Size	0.25 mm × 0.4 mm
Pad Pitch	0.5 mm
Thermal Pad Size	4.7 mm × 4.7 mm
Thermal via Structure	0.25 mm diameter vias on a 0.5 mm grid

Bottom PCB Layer

It is recommended that the bottom thermal pad be thermally connected to a plane. The connection should be direct such that the thermal pad becomes part of the plane.

The use of thermal spokes is not recommended when connecting the thermal pads or via structure to a plane.

Solder Masking

To minimize the formation of solder voids due to solder flowing into the via holes (solder wicking), the via diameter should be small. Optional solder masking of the via holes on the top layer of the PCB plug the via holes, inhibiting solder flow into the holes. To optimize the thermal pad coverage, the solder mask diameter should be no more than 0.1 mm larger than the via hole diameter.

Pads are set by the customer's PCB design rules, and thermal vias are 0.25 mm diameter circular mask, centered on the vias.

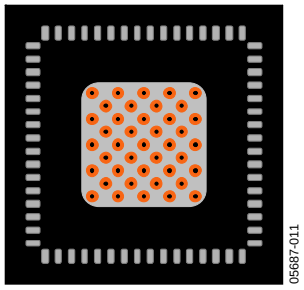


Figure 13. Land Patter—Top PCB Layer

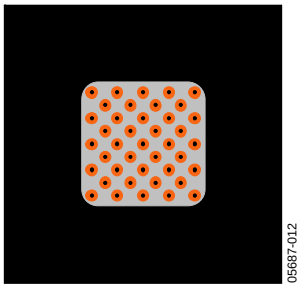


Figure 14. Land Patter—Bottom PCB Layer

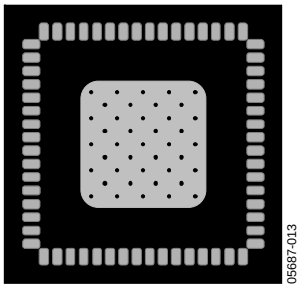


Figure 15. Solder Mask—Top Layer

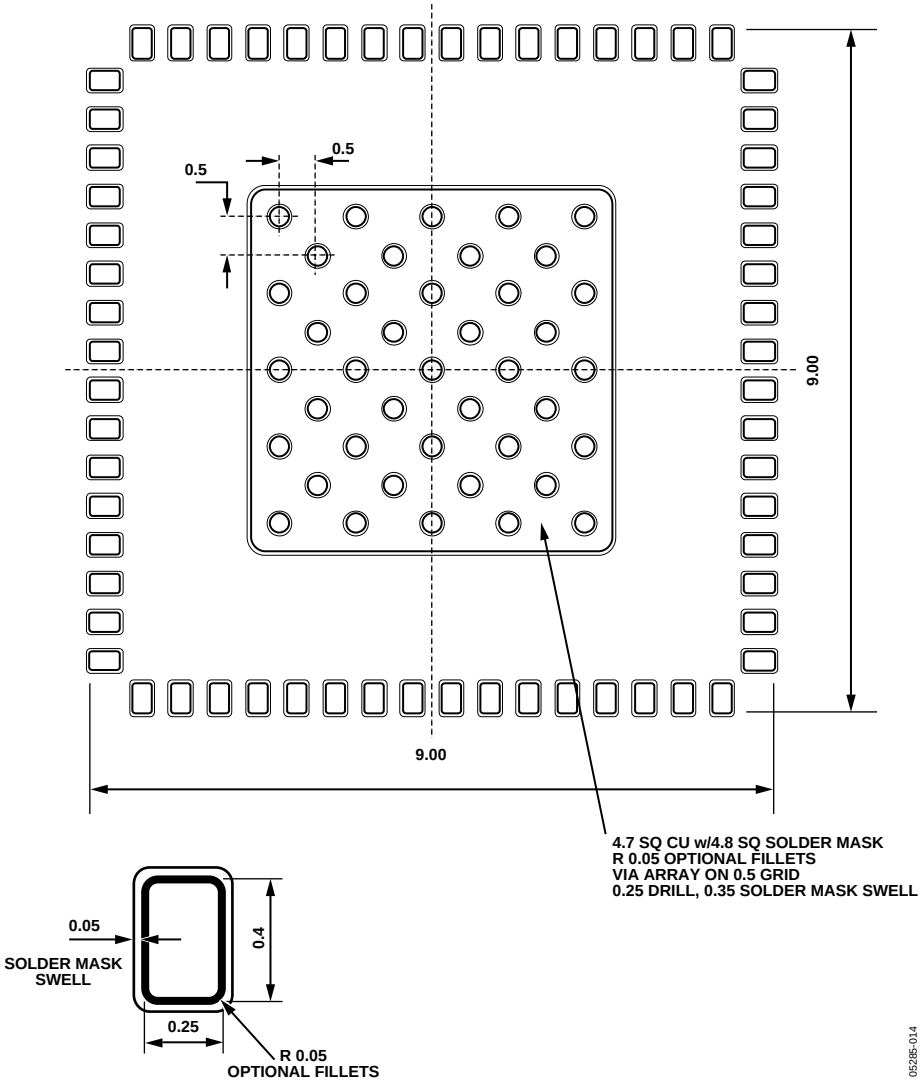
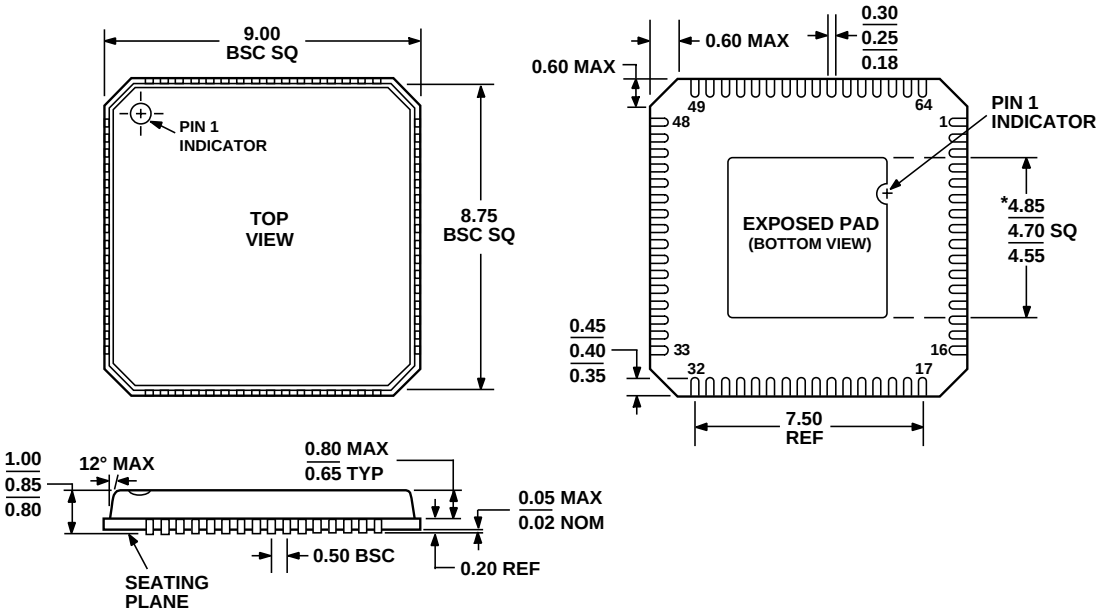


Figure 16. Suggested Land Pattern
Dimensions shown in millimeters

OUTLINE DIMENSIONS



*COMPLIANT TO JEDEC STANDARDS MO-220-VMMD
EXCEPT FOR EXPOSED PAD DIMENSION

Figure 17. 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
9 mm × 9 mm Body, Very Thin Quad (CP-64-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8386JCPZ[1]	0°C to 85°C	64-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-64-1

[1] Z = Pb-free part.

NOTES

D05687–0–8/05(0)