

## **GSM 3 V Receiver IF Subsystem**

AD6458

#### **FEATURES**

Fully Compliant with Standard and Enhanced GSM Specification

- -12 dBm Input 1 dB Compression Point
- -2 dBm Input Third Order Intercept
- 10 dB SSB Noise Figure (330  $\Omega$ )

DC-400 MHz RF and LO Bandwidths

**Linear IF Amplifier** 

Linear-in-dB and Stable over Temperature Voltage Gain Control

**Quadrature Demodulator** 

Onboard Phase-Locked Quadrature Oscillator Demodulates IFs from 5 MHz to 50 MHz

Low Power

9 mA at Midgain

1  $\mu$ A Sleep Mode Operation

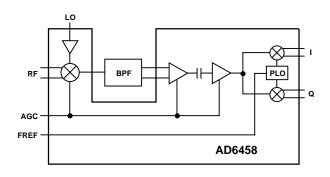
3.0 V to 3.6 V Operation

Interfaces to AD7013, AD7015 and AD6421 Baseband

Converters

20-Lead SSOP

### **FUNCTIONAL BLOCK DIAGRAM**



### **GENERAL DESCRIPTION**

The AD6458 is a 3 V, low power receiver IF subsystem for operation at input frequencies as high as 400 MHz and IFs from 5 MHz up to 50 MHz. It is optimized for operation in GSM, DCS1800 and PCS1900 receivers. It consists of a mixer, IF amplifier, I and Q demodulators, a phase-locked quadrature oscillator, precise AGC subsystem, and a biasing system with external power-down.

The low noise, high intercept mixer of the AD6458 is a doubly-balanced Gilbert cell type. It has a nominal -12 dBm input-referred 1 dB compression point and a -2 dBm input-referred third-order intercept. The mixer section of the AD6458 also includes a local oscillator (LO) preamplifier, which lowers the required LO drive to -16 dBm.

The gain control input accepts an external gain-control voltage input from an external AGC detector or a DAC. It provides an 80 dB gain range with 27 mV/dB gain scaling.

The I and Q demodulators provide inphase and quadrature baseband outputs to interface with Analog Devices' AD7013 (IS54, TETRA, MSAT) and AD7015 and AD6421 (GSM, DCS1800, PCS1900) baseband converters. An onboard

quadrature VCO which is externally phase-locked to the IF signal drives the I and Q demodulators. This locked reference signal is normally provided by an external VCTCXO under the control of the radio's digital processor. The AD6458 can also provide demodulation of N-PSK and N-QAM in many non-TDMA systems when used with external analog carrier recovery systems such as the Costas Loop. Finally, the VCO can be phase-locked to a frequency which is deliberately offset from the IF, as in the case of a Beat-Frequency Oscillator (BFO), resulting in the product detection of CW or SSB.

The AD6458 uses supply voltages from 3.0 V to 3.6 V over the temperature range of  $-40^{\circ}$ C to  $+85^{\circ}$ C. Operation is enabled by a CMOS logical level; response time is typically <80  $\mu$ s. When disabled, the standby current is reduced to 1  $\mu$ A.

The AD6458 comes in a 20-lead shrink small outline (SSOP) surface-mount package.

# $\label{eq:AD6458-SPECIFICATIONS} \textbf{(@ T}_{A} = +25^{\circ}\text{C, V}_{P} = 3.0 \text{ V, GREF} = 1.2 \text{ V, unless otherwise noted)}$

| Parameter   | Conditions  | Min    | Тур   | Max              | Units   |
|---|---|--------|---|------------------|---|
| MIXER  Maximum RF and LO Frequency  AGC Conversion Gain Variation  Input RF Signal Range  Input 1 dB Compression Point  Input Third-Order Intercept  SSB Noise Figure <sup>1</sup> Mixer Output Bandwidth at MXOP   | $\begin{array}{c} 0.2~\mathrm{V} < \mathrm{V_G} < 2.25~\mathrm{V},~\mathrm{Z_S} = 50~\Omega,~\mathrm{Z_{LOAD}} = 330~\Omega \\ \\ @~\mathrm{V_G} = 0.2~\mathrm{V},~\mathrm{Z_S} = 50~\Omega,~\mathrm{Z_{LOAD}} = 330~\Omega \\ @~\mathrm{V_G} = 0.2~\mathrm{V},~\mathrm{Z_S} = 50~\Omega,~\mathrm{Z_{LOAD}} = 330~\Omega \\ @~\mathrm{Z_S} = 1~\mathrm{k}\Omega,~\mathrm{F_{RF}} = 83~\mathrm{MHz},~\mathrm{F_{LO}} = 96~\mathrm{MHz}~\mathrm{at}~-16~\mathrm{dBm} \\ @~-3~\mathrm{dB},~\mathrm{Z_{LOAD}} = 330~\Omega \end{array}$ | -95    | 400<br>-8.5 to +9.5<br>-11<br>-2<br>9<br>55 | -15              | MHz<br>dB<br>dBm<br>dBm<br>dBm<br>dB<br>MHz                               |
| IF AMPLIFIERS AGC Gain Variation Input Referred Noise Input Resistance Bandwidth  | $0.2 \text{ V} < \text{V}_{\text{G}} < 2.25 \text{ V}$ AC Short Circuit Input $\text{@ V}_{\text{G}} = 0.2 \text{ V}$ $\text{@ } -3 \text{ dB}$   |        | -9 to +48<br>3<br>5<br>50                   |                  | dB<br>nV/Hz<br>kΩ<br>MHz  |
| I AND Q DEMODULATORS Demodulation Gain Output Voltage Range Output Voltage Common-Mode Level Output Offset Voltage Output Offset Voltage Variation Output Offset Voltage Variation Error in Quadrature Amplitude Match I/Q Output Bandwidth Output Resistance | IRXP, IRXN, QRXP, QRXN (Not Power Supply Dependant) Differential Differential, over Gain and Temperature Range <sup>2</sup> Differential, for 0.5 V < $V_G$ < 2.4 V and $-25^{\circ}$ C < $T_A$ < +85°C (See Note 2) IF = 13 MHz $C_{LOAD} = 10 \text{ pF}$ Each Pin  | 0.3    | 17 1.5 1 0.5 1.5 0.25 2 4.7                 | $V_P - 0.2$ +150 | $\begin{array}{c} dB \\ V \\ V \\ mV \\ mV \\ \end{array}$                |
| GAIN CONTROL Total Gain Control Range Control Voltage Range at GAIN Gain Scaling Gain Law Conformance Bias Current at GREF Input Resistance at GAIN   | Mixer + IF + Demod, $0.2 \text{ V} < \text{V}_{\text{G}} < 2.25 \text{ V}$  | 0.2 23 | 75<br>27<br>±0.5<br>0.5<br>20               | 2.4<br>32        | $\begin{array}{c} dB \\ V \\ mV/dB \\ dB \\ \mu A \\ k\Omega \end{array}$ |
| PLL Frequency Range Phase Noise Acquisition Time Input Drive Level (FREF)   | IF = 13 MHz, Using Ceramic Filter   | 5      | 0.5<br>80                                   | 40<br>VPOS       | MHz<br>Degree rms<br>μs<br>mV   |
| POWER-DOWN INTERFACE Logical Threshold Input Current for Logical High Turn On Response Time Stand By Current  | Power-Up On Logical High  To Fully Meet Specifications (See Note 3)   |        | 1.5<br>75<br>80<br>1                        | 150<br>8         | V<br>μΑ<br>μs<br>μΑ   |
| POWER SUPPLY Supply Range Worst Case Supply Current Supply Current  | @ $V_{GAIN} = 0.2 \text{ V}$ , $T_A = +85^{\circ}\text{C}$ , $V_P = 3.6 \text{ V}^4$ @ $V_{GAIN} = 1.2 \text{ V}$   | 3.0    | 3.3<br>16.5<br>9                            | 3.6<br>22        | V<br>mA<br>mA   |
| OPERATING TEMPERATURE $T_{MIN}$ to $T_{MAX}$  |   |        | -40 to +85                                  |                  | °C  |

Specifications subject to change without notice.

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 $<sup>^{1}</sup>$ Including IF noise and using 13 MHz ceramic filter, at  $V_{GAIN}$  = 0.2 V.  $^{2}$ Histograms of Demodulator Offset Voltage Variation in Gain and Temperature can be found in Figures 23 to 27.

<sup>&</sup>lt;sup>3</sup>Max value represent the value at six times the standard deviation, in the worst case condition (T<sub>A</sub> = +85°C). The value at three times the standard deviation is 5 µA.

<sup>&</sup>lt;sup>4</sup>Max value represent the value at six times the standard deviation. The value at three times the standard variation is 19 mA.

### ABSOLUTE MAXIMUM RATINGS1

Supply Voltage VPS1, VPS2 to COM1, COM2 .... +3.6 V Internal Power Dissipation  $^2$  .... 600 mW Operating Temperature Range ....  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  Storage Temperature Range ....  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$  Lead Temperature, Soldering (60 sec) ....  $+300^{\circ}\text{C}$ 

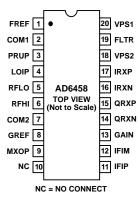
#### NOTES

<sup>1</sup>Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended rating conditions for extended periods may affect device reliability.

### **ORDERING GUIDE**

|           | Temperature    | Package                      | Package |
|-----------|----------------|------------------------------|---------|
|           | Range          | Description                  | Option  |
| AD6458ARS | –40°C to +85°C | 20-Lead Shrink Small Outline | RS-20   |

### PIN CONNECTION 20-Lead SSOP (RS-20)



### PIN FUNCTION DESCRIPTIONS

| Pin<br>Number | Pin<br>Label | Description               | Function  |
|---------------|--------------|---------------------------|---|
| 1             | FREF         | Frequency Reference Input | Demodulation LO Input. May be 3 V CMOS input or >100 mV ac coupled for lowest stand by current. |
| 2             | COM1         | Common 1                  | Ground.   |
| 3             | PRUP         | Power-Up Input            | CMOS compatible power up control; $0 = OFF$ , $3 V = ON$ .                                      |
| 4             | LOIP         | Local Oscillator Input    | AC coupled LO input. Only 50 mV drive needed, 500 mV max.                                       |
| 5             | RFLO         | RF "Low" Input            | Usually connected to ac ground.   |
| 6             | RFHI         | RF "High" Input           | AC coupled, $-109$ dBV to $-29$ dBV RF input from 1 k $\Omega$ filter for optimal operation.    |
| 7             | COM2         | Common 2                  | Ground.   |
| 8             | GREF         | Gain Reference Input      | High impedance input, sets gain scaling, typically 1.2 V.                                       |
| 9             | MXOP         | Mixer Output              | Output of the Mixer.  |
| 10            | NC           |                           | Not internally connected. Should be grounded.   |
| 11            | IFIP         | IF Input "Plus"           | Differential Input of variable gain amplifier.  |
| 12            | IFIM         | IF Input "Minus"          | Differential Input of variable gain amplifier.  |
| 13            | GAIN         | Gain Control Input        | 0.2 V-2.4 V using 3 V supply. Max gain at 0.2 V.  |
| 14            | QRXN         | Q Output "Negative"       | Differential Q Output.  |
| 15            | QRXP         | Q Output "Positive"       | Differential Q Output.  |
| 16            | IRXN         | I Output "Negative"       | Differential I Output.  |
| 17            | IRXP         | I Output "Positive"       | Differential I Output.  |
| 18            | VPS2         | VPOS Supply 2             | Supply Voltage.   |
| 19            | FLTR         | PPL Loop Filter           | Series RC loop filter, connected to VPS2.   |
| 20            | VPS1         | VPOS Supply 1             | Supply Voltage.   |

### CAUTION\_

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD6458 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



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 $<sup>^2</sup>$ Thermal Characteristics: 20-Lead SSOP Package:  $\theta_{JA}$  = 126 $^{\circ}$ C/W.

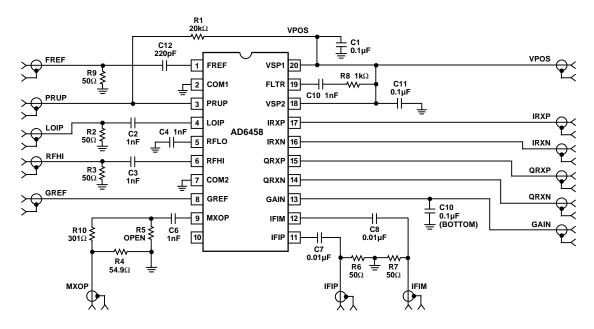


Figure 1. Characterization Board

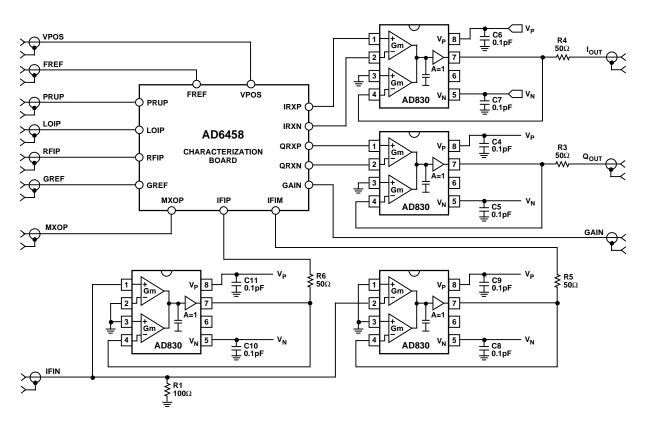


Figure 2. Characterization Test Set

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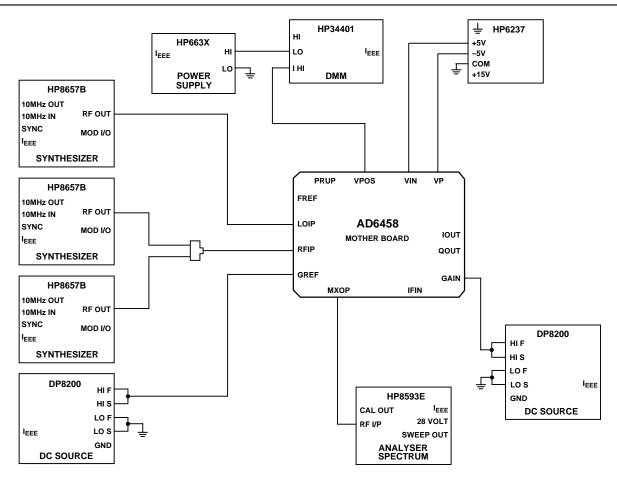


Figure 3. Mixer Characterization Setup

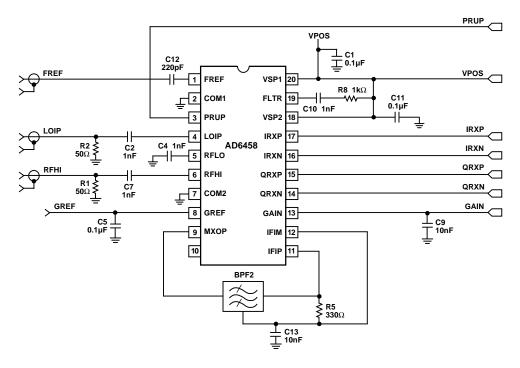


Figure 4. Typical Connection Diagram

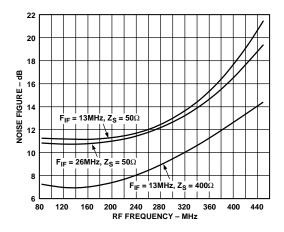


Figure 5. Mixer Noise Figure vs. RF Frequency

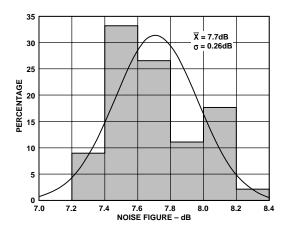


Figure 6. Mixer Noise Figure Histogram,  $R_S = 1 \text{ k}\Omega$ ,  $F_{RF} = 83 \text{ MHz}$ ,  $F_{IF} = 13 \text{ MHz}$ 

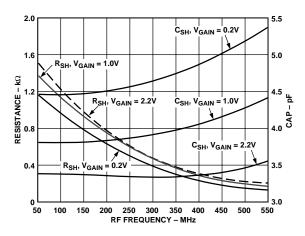


Figure 7. Mixer Input Impedance vs. RF Frequency,  $V_{POS} = 3.0 \text{ V}$ ,  $T_A = +25^{\circ}\text{C}$ 

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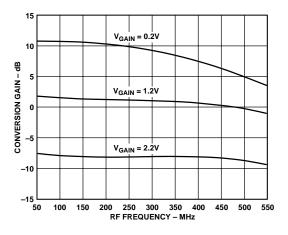


Figure 8. Mixer Conversion Gain vs. RF Frequency,  $T_A = +25^{\circ}C$ ,  $V_{POS} = 3.0$  V,  $V_{REF} = 1.2$  V,  $F_{IF} = 13$  MHz

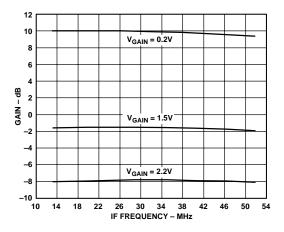


Figure 9. Mixer Conversion Gain vs. IF Frequency,  $T_A = +25^{\circ}C$ ,  $V_{POS} = 3$  V,  $V_{REF} = 1.2$  V,  $F_{RF} = 250$  MHz

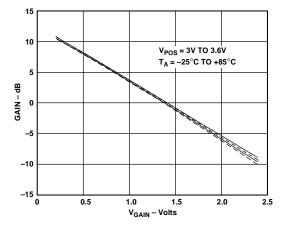


Figure 10. Mixer Conversion Gain vs  $V_{GAIN}$ ,  $V_{REF} = 1.2 \text{ V}$ ,  $F_{IF} = 13 \text{ MHz}$ ,  $F_{RF} = 83 \text{ MHz}$ 

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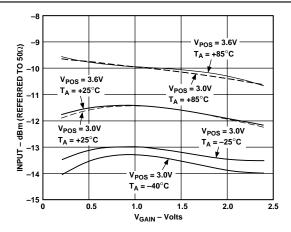


Figure 11. Mixer Input 1 dB Compression Point vs.  $V_{GAIN}$ ,  $V_{REF} = 1.2 \text{ V}$ ,  $F_{RF} = 83 \text{ MHz}$ ,  $F_{IF} = 13 \text{ MHz}$ 

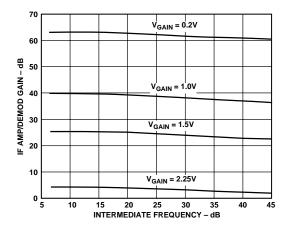


Figure 12. IF Amplifier and Demodulator Gain vs. Frequency,  $T_A = +25$ °C,  $V_{POS} = 3.0$  V,  $V_{REF} = 1.2$  V

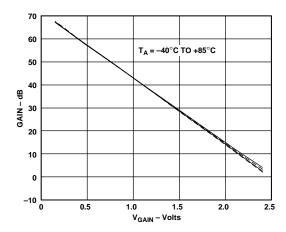


Figure 13. IF Amplifier and Demodulator Gain vs.  $V_{GAIN}$ ,  $T_A = +25$ °C,  $V_{POS} = 3.0$  V,  $F_{IF} = 13$  MHz,  $V_{REF} = 1.2$  V

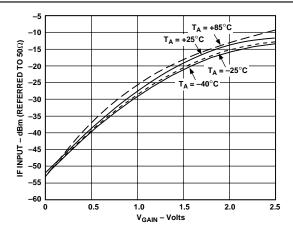


Figure 14. IF Amplifier/Demodulator Input 1 dB Compression Point vs.  $V_{GAIN}$ ,  $F_{IF}$  = 13 MHz,  $V_{REF}$  = 1.2 V,  $T_A$  = +25°C,  $V_{POS}$  = 3.0 V

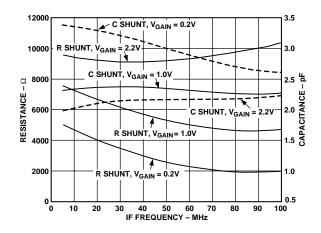


Figure 15. IF Amplifier Input Impedance vs. Frequency,  $T_A = +25^{\circ}C$ ,  $V_{POS} = 3.0~V$ ,  $V_{REF} = 1.2~V$ 

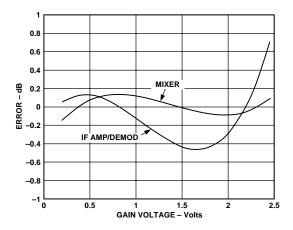


Figure 16. AD6458 Gain Error vs. Gain Control Voltage, Representative Part

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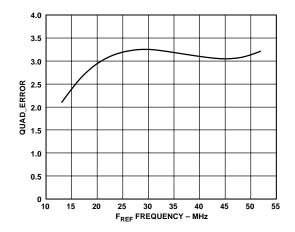


Figure 17. Demodulator Quadrature Error vs.  $F_{REF}$ Frequency,  $T_A = +25^{\circ}C$ ,  $V_{POS} = 3.0 \text{ V}$ 

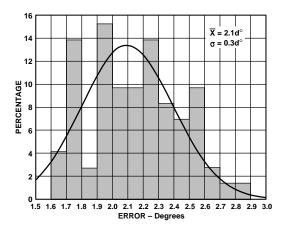


Figure 18. Demodulator Quadrature Error Histogram  $T_A = +25^{\circ}C$ ,  $V_{POS} = 3.0 \text{ V}$ .  $F_{IF} = 13 \text{ MHz}$ 

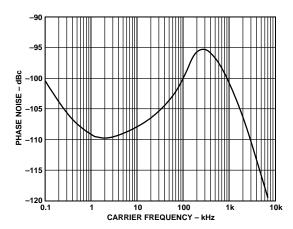


Figure 19. PLL Phase Noise vs. Frequency,  $V_{POS} = 3 V$ ,  $C_{FLTR} = 1 \text{ nF}$ ,  $R_{FLTR} = 1 \text{ k}\Omega$ ,  $F_{REF} = 13 \text{ MHz}$ 

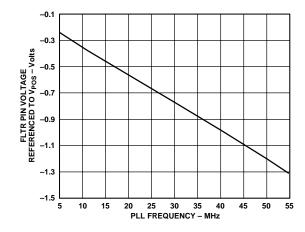


Figure 20. PLL Loop Voltage at FLTR Pin (kVCO) vs. Frequency

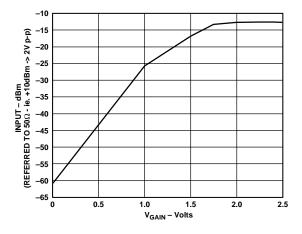


Figure 21. System [(Mixer + IF Ceramic Filter + IF Amplifier + Demodulator)] Input 1 dB Compression Point vs.  $V_{GAIN}$ ,  $T_A = +25$ °C,  $V_{POS} = 3.0$  V,  $F_{IF} = 13$  MHz,  $F_{RF} = 83$  MHz,  $V_{REF} = 1.2$  V

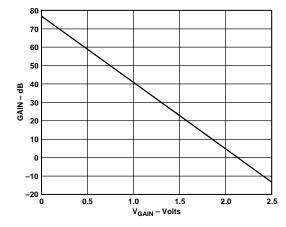


Figure 22. System (Mixer + IF Ceramic Filter + IF Amplifier + Demodulator) Conversion Gain vs.  $V_{GAIN}$ ,  $T_A = +25^{\circ}C$ ,  $V_{POS} = 3.0 \text{ V}$ ,  $F_{IF} = 13 \text{ MHz}$ ,  $F_{RF} = 83 \text{ MHz}$ ,  $V_{REF} = 1.2 \text{ V}$ 

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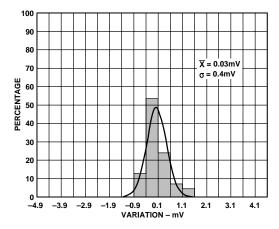


Figure 23. Demodulation Output Offset Voltage Variation Histogram with Variation Referred to Offset at  $V_{GAIN}=1.2~V$  and  $T_A=+25^{\circ}C$ ,  $V_{GAIN}=2.25~V$  and  $T_A=+25^{\circ}C$ 

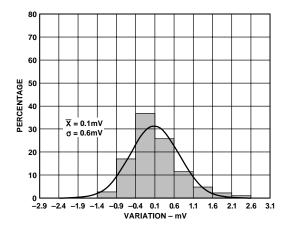


Figure 24. Demodulation Output Offset Voltage Variation Histogram with Variation Referred to Offset at  $V_{GAIN}=1.2~V$  and  $T_A=+25^{\circ}C$ ,  $V_{GAIN}=0.5~V$  and  $T_A=+25^{\circ}C$  C

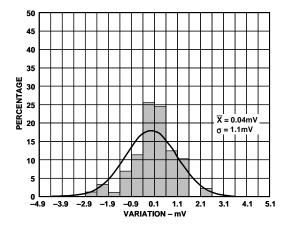


Figure 25. Demodulation Output Offset Voltage Variation Histogram with Variation Referred to Offset at  $V_{GAIN}$  = 1.2 V and  $T_A$  = +25°C,  $V_{GAIN}$  = 0.2 V and  $T_A$  = +25°C

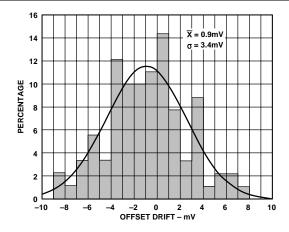


Figure 26. Demodulation Output Offset Voltage Variation Histogram with Variation Referred to Offset at  $V_{GAIN}$  = 1.2 V and  $T_A$  = +25°C,  $V_{GAIN}$  = 0.2 V and  $T_A$  = -25°C

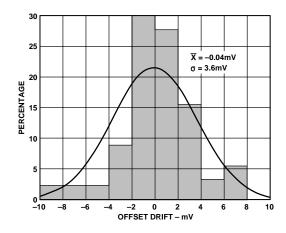


Figure 27. Demodulation Output Offset Voltage Variation Histogram with Variation Referred to Offset at  $V_{GAIN}$  = 1.2 V and  $T_A$  = +25°C,  $V_{GAIN}$  = 0.2 V and  $T_A$  = +85°C

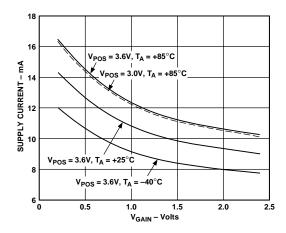


Figure 28. Power Supply Current vs. Gain Control Voltage,  $V_{REF} = 1.2 \text{ V}$ 

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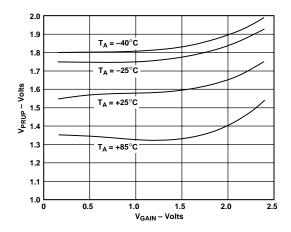


Figure 29. Minimum Power-Up Voltage vs  $V_{GAIN}$ ,  $V_{POS}$  = 3.0 V,  $V_{REF}$  = 1.2 V

### PRODUCT OVERVIEW

The AD6458 provides most of the active circuitry required to realize a complete low power, single-conversion superheterodyne receiver, or the latter part of a double-conversion receiver, at input frequencies up to 400 MHz, with an IF from 5 MHz to 50 MHz. The internal I/Q demodulators, and their associated phase-locked loop, support a wide variety of modulation modes, including n-PSK, n-QAM, and GMSK. A single positive supply voltage of 3.3 V is required (3.0 V minimum, 3.6 V maximum) at a typical supply current of 9 mA at midgain. In the following discussion,  $V_{\rm POS}$  will be used to denote the power supply voltage, which will be assumed to be 3.3 V.

Figure 31 shows the main sections of the AD6458. It consists of a variable-gain UHF mixer and linear two-stage IF strip, which together provide a calibrated voltage-controlled gain range of more than 76 dB, followed by dual quadrature demodulators. These are driven by inphase and quadrature clocks generated by a Phase-Locked Loop (PLL), which is locked to a corrected external reference. A CMOS-compatible power-down interface completes the AD6458.

#### Mixer

The UHF mixer is an improved Gilbert-cell design, and can operate from low frequencies (it is internally dc-coupled) up to an RF input of 400 MHz. The dynamic range at the input of the mixer is determined at the upper end by the maximum input signal level of  $\pm 56$  mV (–15 dBm in 50  $\Omega$  between RFHI and RFLO) up to which the mixer remains linear and, at the lower end, by the noise level. It is customary to define the linearity of a mixer in terms of the 1 dB gain-compression point and third-order intercept, which for the AD6458 are –12 dBm and –2 dBm, respectively, in a 50  $\Omega$  system.

The mixer's RF input port is differential; that is, pin RFLO is functionally identical to RFHI, and these nodes are internally biased. The RF port can be modeled as a parallel RC circuit as shown in Figure 30.

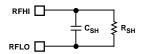


Figure 30. Mixer Port Modeled as a Parallel RC Network

The local oscillator (LO) input is internally biased at  $V_P-0.8~V$  and must be ac coupled. The LO interface includes a preamplifier which minimizes the drive requirements, thus simplifying the oscillator design and reducing LO leakage from the RF port. The LO requires a single-sided drive of  $\pm 50~mV$ , or -16~dBm in a  $50~\Omega$  system. For operation above 300 MHz noise figure can be improved by increasing the LO level.

The output of the mixer is single ended with a 330  $\Omega$  impedance for driving ceramic filters.

The conversion gain is measured between the mixer input and the input of this filter, and varies between -9 dB and +10 dB as a function of the voltage at Pin GAIN.

The maximum permissible signal level at Pin MXOP is determined by the maximum gain control voltage.

The mixer output port is shown in Figure 32.

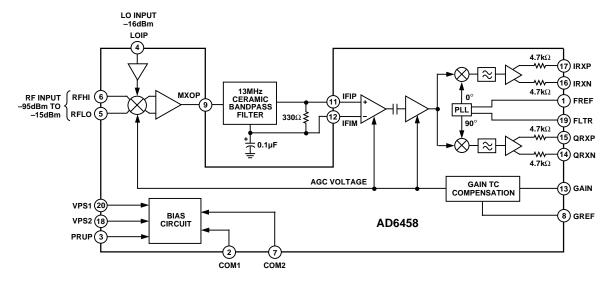


Figure 31. Functional Block Diagram

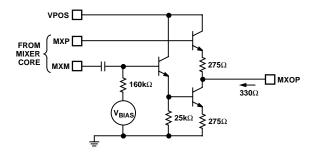


Figure 32. Mixer Output Port

### IF Amplifier

Most of the gain in the AD6458 resides in the IF amplifier strip, which comprises two stages. Both are fully differential and each has a gain span of 26 dB for the AGC voltage range of 0.2 V to 2.25 V. Thus, in conjunction with the variable gain of the mixer, the total gain span is 76 dB. The overall IF gain varies from –9 dB to 48 dB for the nominal AGC voltage of 0.2 V to 2.25 V. Maximum gain is at  $V_{GAIN} = 0.2$  V.

The IF input is differential at IFIP and IFIM. Figure 33 shows a simplified schematic of the IF interface modeled as parallel RC network.

The IF's small-signal bandwidth is approximately 50 MHz from IFIP and IFIM through the demodulator.

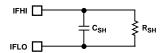


Figure 33. IF Amplifier Port Modeled as a Parallel RC Network

### **Gain Scaling**

The AD6458's overall gain, expressed in decibels, is linear with respect to the AGC voltage  $V_{GAIN}$  at pin GAIN. The gain of all sections is maximum when  $V_{GAIN}$  is 0.2, and falls off as the bias is increased to  $V_{GAIN} = 2.25$  and is independent of the power supply voltage. The gain of all stages changes simultaneously. The AD6458's gain scaling is also temperature compensated.

The GAIN pin of the AD6458 is an input driven by an external low impedance voltage source, normally a DAC, under the control of radio's digital processor.

The gain-control scaling is directly proportional to the reference voltage applied to the pin GREF and is independent of the power supply voltage. When this input is set to the nominal value of 1.2 V, the scale is nominally 27 mV/dB (37 dB/V). Under these conditions, 76 dB of gain range (mixer plus IF) corresponds to a control voltage of 0.2 V <=  $V_G$  <= 2.25 V. The final centering of this 2.05 V range depends on the insertion losses of the IF filters used.

Pin GREF can be tied to an external voltage reference,  $V_{REF}$ , provided, for example, by a AD1580 (1.21 V) voltage reference.

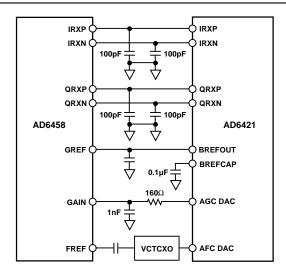


Figure 34. Interfacing the AD6458 to the AD6421 Baseband Converter

When using the Analog Devices AD7013 (IS54, TETRA and satellite receiver applications) and AD7015 or AD6421 (GSM, DCS1800, PCS1900) baseband converters, the external reference may also be provided by the reference output of the baseband converters. The interface between the AD6458 and the AD6421 baseband converter is shown in Figure 34. The AD6421 baseband converter provides a V<sub>REF</sub> of 1.23 V; an auxiliary DAC in the AD6421 can be used to generate the AGC voltage. Since it uses the same reference voltage, the numerical input to this DAC provides an accurate RSSI value in digital form, no longer requiring the reference voltage to have high absolute accuracy.

### I/Q Demodulators

Both demodulators (I and Q) receive their inputs internally from the IF amplifiers. Each demodulator comprises a full-wave synchronous detector followed by an 8 MHz, two-pole low-pass filter, producing differential outputs at pins IRXP and IRXN, and QRXP and QRXN. Using the I and Q demodulators for IFs above 50 MHz is precluded by the 5 MHz to 50 MHz range of the PLL used in the demodulator section.

The I and Q outputs are differential and can swing up to 2.2 V p-p at the low supply voltage of 3.0 V. They are nominally centered at 1.5 V independently of power supply. They can therefore directly drive the RX ADCs in the AD6421 baseband converter, which require an amplitude of 1.23 V to fully load them when driven by a differential signal. The conversion gain of the I and Q demodulators is 17 dB.

For IFs of less than 8 MHz, the on-chip low-pass filters (8 MHz cutoff) do not adequately attenuate the IF or feedthrough products; the maximum input voltage must thus be limited to allow sufficient headroom at the I and Q outputs, not only for the desired baseband signal but also the unattenuated higher order demodulation products. These products can be removed by an external low-pass filter. A simple 1-pole RC filter, with its corner above the modulation bandwidth, is sufficient to attenuate undesired outputs. The design of the RC filter is eased by the  $4.7~\mathrm{k}\Omega$  resistor integrated at each I and Q output pin.

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### I/Q Convention

The AD6458 is a complete IF receive subsystem. Although not a requirement for using the AD6458, most applications will use a high-side LO injection on pin LOIP (Pin 4) of the mixer. The I and Q convention is such that when a spectrum with I leading Q is presented to the input of the mixer, and a high-side LO is presented on pin LOIP, I still leads Q at the baseband output of the AD6458.

#### Phase-Locked Loop

The demodulators are driven by quadrature signals provided by a variable frequency quadrature oscillator (VFQO), phase-locked to a reference signal applied to Pin FREF. When this signal is at the IF, in-phase and quadrature baseband outputs are generated at the I output (IRXP and IRXN) and Q output (QRXP and QRXN), respectively. The quadrature accuracy of this VFQO is typically 2° at 13 MHz. A simplified diagram of the FREF input is shown in Figure 35.

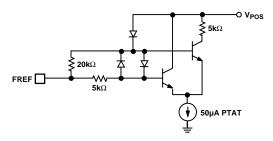


Figure 35. Simplified Schematic of the FREF Interface

The VFQO operates from 5 MHz to 50 MHz and is controlled by the voltage between  $V_{POS}$  and FLTR. In normal operation, a series RC network, forming the PLL loop filter, is connected from FLTR to  $V_{POS}$ . The use of an integral sample-hold system ensures that the frequency-control voltage on pin FLTR remains held during power-down, so reacquisition of the carrier occurs in less than 80  $\mu$ s.

In practice, the probability of a phase mismatch at power-up is high, so the worst-case linear settling period to full lock needs to be considered in making filter choices. This is typically < 80  $\mu s$  for a quadrature phase error of  $\pm 3^{\circ}$  at an IF of 13 MHz. Note that the VFQO always provides quadrature between its own I and Q outputs, but the phasing between it and the reference carrier will swing around the final value during the PLL's settling time.

### **Bias System**

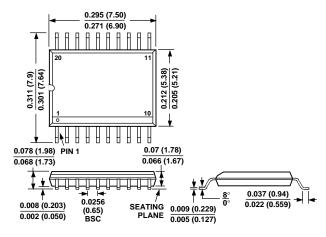
The AD6458 operates from a single supply,  $V_{POS}$ , usually 3.3 V, at a typical supply current of 9 mA at midgain and  $T_A = +25^{\circ}C$ . Any voltage from 3.0 V to 3.6 V may be used.

The bias system includes a fast acting active high CMOS-compatible power-up switch, allowing the part to idle at 1  $\mu$ A when disabled. Biasing is generally proportional-to-absolute-temperature (PTAT) to ensure stable gain with temperature. Other special biasing techniques are used to ensure very accurate gain, stable over the full temperature range.

### **OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).

### 20-Lead Plastic SSOP (RS-20)



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