2 ADC, 8 DAC, 96 kHz, 24-Bit Σ-Δ Codec

Preliminary Technical Data — AD1835

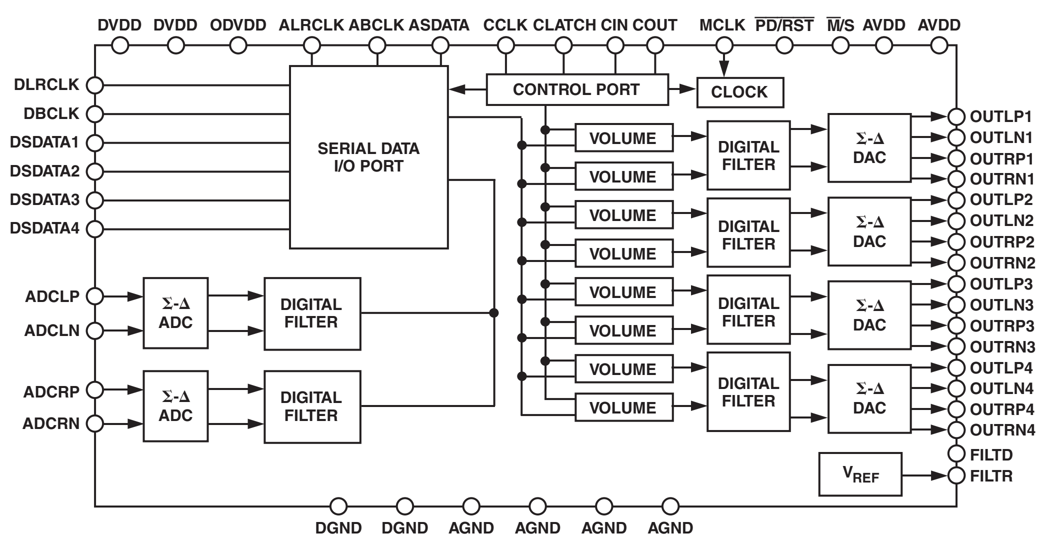
FEATURES
- 5 V Stereo Audio System with 3.3 V Tolerant Digital Interface
- Supports up to 96 kHz Sample Rates
- 192 kHz Sample Rate Available on One DAC
- Supports 16-/20-/24-Bit Word Lengths
- Multibit Sigma-Delta Modulators with "Perfect Differential Linearity Restoration" for Reduced Idle Tones and Noise Floor
- Data Directed Scrambling DACs—Least Sensitive to Jitter
- Differential Output for Optimum Performance
  - ADCs: –92 dB THD + N, 100 dB SNR, and Dynamic Range
  - DACs: –95 dB THD + N, 110 dB SNR, and Dynamic Range
- On-Chip Volume Controls per Channel with 1024-Step Linear Scale
- DAC and ADC Software Controllable Clickless Mutes
- Digital De-Emphasis Processing
- Supports 256 × f_S, 512 × f_S, and 768 × f_S Master Mode Clocks
- Power-Down Mode Plus Soft Power-Down Mode
- Flexible Serial Data Port with Right-Justified, Left-Justified, I²S-Compatible, and DSP Serial Port Modes
- TDM Interface Mode Supports 8 In/8 Out Using a Single SHARC® SPORT
- 52-Lead MQFP Plastic Package

APPLICATIONS
- DVD Video and Audio Players
- Home Theater Systems
- Automotive Audio Systems
- Audio/Visual Receivers
- Digital Audio Effects Processors

PRODUCT OVERVIEW
The AD1835 is a high-performance, single-chip codec featuring four stereo DACs and one stereo ADC. Each DAC comprises a high-performance digital interpolation filter, a multibit sigma-delta modulator featuring Analog Devices' patented technology,

(Continued on Page 11)

FUNCTIONAL BLOCK DIAGRAM



SHARC is a registered trademark of Analog Devices, Inc.

REV. PrA

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

AD1835–SPECIFICATIONS

TEST CONDITIONS

Supply Voltages (AV_{DD}, DV_{DD})	5.0 V
Ambient Temperature	25°C
Input Clock	12.288 MHz, (256 × f_S Mode)
ADC Input Signal	1.0078125 kHz, –1 dBFS (Full Scale)
DAC Input Signal	1.0078125 kHz, 0 dBFS (Full Scale)
Input Sample Rate (f_S)	48 kHz
Measurement Bandwidth	20 Hz to 20 kHz
Word Width	24 Bits
Load Capacitance	100 pF
Load Impedance	47 kΩ

Performance of all channels is identical (exclusive of the Interchannel Gain Mismatch and Interchannel Phase Deviation specifications).

Parameter	Min	Typ	Max	Unit
ANALOG-TO-DIGITAL CONVERTERS				
ADC Resolution		24		Bits
Dynamic Range (20 Hz to 20 kHz, –60 dB Input)				
No Filter	100	103		dB
A-Weighted	101	105		dB
Total Harmonic Distortion + Noise (THD + N)		–93	–88.5	dB
Interchannel Isolation		100		dB
Interchannel Gain Mismatch		0.01		dB
Analog Inputs				
Differential Input Range (± Full Scale)	–2.828		+2.828	V
Common-Mode Input Volts		2.25		V
Input Impedance		4		kΩ
Input Capacitance		15		pF
V_{REF}		2.25		V
DC Accuracy				
Gain Error		+5		%
Gain Drift		TBD		ppm/°C
Crosstalk (EIAJ Method)		TBD		dB
DIGITAL-TO-ANALOG CONVERTERS				
DAC Resolution				
Dynamic Range (20 Hz to 20 kHz, –60 dBFS Input)				
No Filter	103	105		
With A-Weighted Filter	105	108		dB
Total Harmonic Distortion + Noise		–95	–90	dB
Interchannel Isolation		100		dB
DC Accuracy				
Gain Error		±4.0		%
Interchannel Gain Mismatch		0.01		%
Gain Drift		150		ppm/°C
Interchannel Crosstalk (EIAJ method)		–120		dB
Interchannel Phase Deviation		±0.1		Degrees
Volume Control Step Size (1023 Linear Steps)		0.098		%
Volume Control Range (Max Attenuation)		60		dB
Mute Attenuation		–100		dB
De-Emphasis Gain Error		±0.1		dB
Full-Scale Output Voltage at Each Pin (Single-Ended)		1.0 (2.8)		Vrms (V p-p)
Output Resistance at Each Pin		115		Ω
Common-Mode Output Volts		2.25		V
ADC DECIMATION FILTER, 48 kHz*				
Pass Band		20		kHz
Pass-Band Ripple		±0.01		dB
Stop Band		24		kHz
Stop-Band Attenuation		120		dB
Group Delay		910		µs

Parameter	Min	Typ	Max	Unit
ADC DECIMATION FILTER, 96 kHz*				
Pass Band		40		kHz
Pass-Band Ripple		±0.01		dB
Stop Band		48		kHz
Stop-Band Attenuation		120		dB
Group Delay		460		µs
DAC INTERPOLATION FILTER, 48 kHz*				
Pass Band			20	kHz
Pass-Band Ripple		±0.01		dB
Stop Band	24			kHz
Stop-Band Attenuation	55			dB
Group Delay		340		µs
DAC INTERPOLATION FILTER, 96 kHz*				
Pass Band			37.5	kHz
Pass-Band Ripple		±0.01		dB
Stop Band	55.034			kHz
Stop-Band Attenuation	55			dB
Group Delay		160		µs
DAC INTERPOLATION FILTER, 192 kHz*				
Pass Band			89.954	kHz
Pass-Band Ripple		±0.01		dB
Stop Band	104.85			kHz
Stop-Band Attenuation	80			dB
Group Delay		110		µs
DIGITAL I/O				
Input Voltage High	2.4			V
Input Voltage Low			0.8	V
Output Voltage High		ODV_{DD} – 0.4		V
Output Voltage Low			0.4	V
Leakage Current			±10	µA
POWER SUPPLIES				
Supply Voltage (AV_{DD} and DV_{DD})	4.5	5.0	5.5	V
Supply Voltage (OV_{DD})	3.0		DV_{DD}	V
Supply Current I_{ANALOG}		84	95	mA
Supply Current I_{ANALOG}, Power-Down		55	67	mA
Supply Current $I_{DIGITAL}$		64	72	mA
Supply Current $I_{DIGITAL}$, Power-Down		1	4	mA
Dissipation				
Operation, Both Supplies		740		mW
Operation, Analog Supply		420		mW
Operation, Digital Supply		320		mW
Power-Down, Both Supplies		280		mW
Power Supply Rejection Ratio				
1 kHz, 300 mV p-p Signal at Analog Supply Pins		–60		dB
20 kHz, 300 mV p-p Signal at Analog Supply Pins		–50		dB

*Guaranteed by design.

Specifications subject to change without notice.

AD1835–SPECIFICATIONS

TIMING

Parameter		Min	Max	Unit	Comments
MASTER CLOCK AND RESET					
t_{MH}	MCLK High	15		ns	
t_{ML}	MCLK Low	15		ns	
t_{PDR}	PD/RST Low	20		ns	
SPI PORT					
t_{CCH}	CCLK High	40		ns	
t_{CCL}	CCLK Low	40		ns	
t_{CCP}	CCLK Period	80		ns	
t_{CDS}	CDATA Setup	10		ns	To CCLK Rising
t_{CDH}	CDATA Hold	10		ns	From CCLK Rising
t_{CLS}	CLATCH Setup	10		ns	To CCLK Rising
t_{CLH}	CLATCH Hold	10		ns	From CCLK Rising
t_{COE}	COUT Enable		15	ns	From CLATCH Falling
t_{COD}	COUT Delay		20	ns	From CCLK Falling
t_{COTS}	COUT Three-State		25	ns	From CLATCH Rising
DAC SERIAL PORT					
Normal Mode (Slave)					
t_{DBH}	DBCLK High	60		ns	
t_{DBL}	DBCLK Low	60		ns	
f_{DB}	DBCLK Frequency	$64 \times f_S$			
t_{DLS}	DLRCLK Setup	10		ns	To DBCLK Rising
t_{DLH}	DLRCLK Hold	10		ns	From DBCLK Rising
t_{DDS}	DSDATA Setup	10		ns	To DBCLK Rising
t_{DDH}	DSDATA Hold	10		ns	From DBCLK Rising
Packed 256 Modes (Slave)					
t_{DBH}	DBCLK High	15		ns	
t_{DBL}	DBCLK Low	15		ns	
f_{DB}	DBCLK Frequency	$256 \times f_S$			
t_{DLS}	DLRCLK Setup	10		ns	To DBCLK Rising
t_{DLH}	DLRCLK Hold	5		ns	From DBCLK Rising
t_{DDS}	DSDATA Setup	10		ns	To DBCLK Rising
t_{DDH}	DSDATA Hold	10		ns	From DBCLK Rising
ADC SERIAL PORT					
Normal Mode (Master)					
t_{ABD}	ABCLK Delay		25	ns	From MCLK Rising Edge
t_{ALD}	ALRCLK Delay Low		5	ns	From ABCLK Falling Edge
t_{ABDD}	ASDATA Delay		10	ns	From ABCLK Falling Edge
Normal Mode (Slave)					
t_{ABH}	ABCLK High	60		ns	
t_{ABL}	ABCLK Low	60		ns	
f_{AB}	ABCLK Frequency	$64 \times f_S$			
t_{ALS}	ALRCLK Setup	5		ns	To ABCLK Rising
t_{ALH}	ALRCLK Hold	15		ns	From ABCLK Rising
Packed 256 Mode (Master)					
t_{PABD}	ABCLK Delay		20	ns	From MCLK Rising Edge
t_{PALD}	LRCLK Delay		5	ns	From ABCLK Falling Edge
t_{PABDD}	ASDATA Delay		10	ns	From ABCLK Falling Edge

Parameter		Min	Max	Unit	Comments
TDM256 MODE (Master)					
t_{TBD}	BCLK Delay		20	ns	From MCLK Rising
t_{FSD}	FSTDM Delay		5	ns	From BCLK Rising
t_{TABDD}	ASDATA Delay		10	ns	From BCLK Rising
t_{TDDS}	DSDATA1 Setup	15		ns	To BCLK Falling
t_{TDDH}	DSDATA1 Hold	15		ns	From BCLK Falling
TDM256 MODE (Slave)					
f_{AB}	BCLK Frequency	$256 \times f_S$		ns	
t_{TBCH}	BCLK High	min		ns	
t_{TBCL}	BCLK Low	min		ns	
t_{TFS}	FSTDM Setup	min		ns	To BCLK Falling
t_{TFH}	FSTDM Hold	min		ns	From BCLK Falling
t_{ABDD}	ASDATA Delay		max	ns	From BCLK Rising
t_{TDDS}	DSDATA1 Setup	min		ns	To BCLK Falling
t_{TDDH}	DSDATA1 Hold	min		ns	From BCLK Falling
TDM512 MODE (Master)					
t_{ABDH}	BCLK Delay		40	ns	From MCLK Rising
t_{FSD}	FSTDM Delay		5	ns	From BCLK Rising
t_{TABDD}	ASDATA Delay		10	ns	From BCLK Rising
t_{TDDS}	DSDATA1 Setup	15		ns	To BCLK Falling
t_{TDDH}	DSDATA1 Hold	15		ns	From BCLK Falling
TDM512 MODE (Slave)					
f_{AB}	BCLK Frequency	$512 \times f_S$			
t_{TBCH}	BCLK High	20		ns	
t_{TBCL}	BCLK Low	20		ns	
t_{TFS}	FSTDM Setup	5		ns	To BCLK Rising
t_{TFH}	FSTDM Hold	10		ns	From BCLK Rising
t_{TABDD}	ASDATA Delay		20	ns	From BCLK Rising
t_{TDDS}	DSDATA1 Setup	5		ns	To BCLK Rising
t_{TDDH}	DSDATA1 Hold	10		ns	From BCLK Rising
AUXILIARY INTERFACE					
t_{AXDS}	AAUXDATA Setup	10		ns	To AUXBCLK Rising
t_{AXDH}	AAUXDATA Hold	10		ns	From AUXBCLK Rising
f_{ABP}	AUXBCLK Frequency	$64 \times f_S$			
Slave Mode					
t_{AXBH}	AUXBCLK High	15		ns	
t_{AXBL}	AUXBCLK Low	15		ns	
t_{AXLS}	AUXLRCLK Setup	10		ns	To AUXBCLK Rising
t_{AXLH}	AUXLRCLK Hold	10		ns	From AUXBCLK Rising
Master Mode					
$t_{AUXLRCLK}$	AUXLRCLK Delay	5		ns	From AUXBCLK Falling
$t_{AUXBCLK}$	AUXBCLK Delay	15		ns	From MCLK Rising Edge

Specifications subject to change without notice.

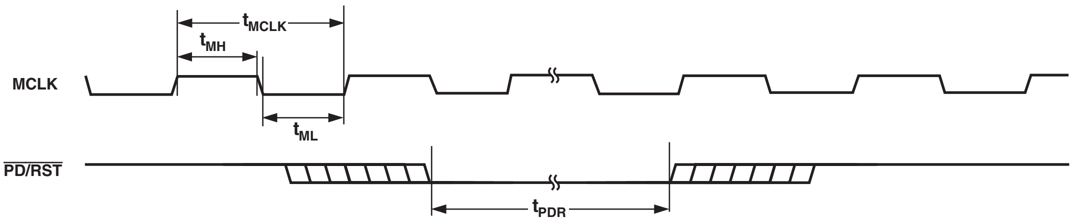


Figure 1. MCLK and $\overline{\text{PD/RST}}$ Timing

TEMPERATURE RANGE

Parameter	Min	Typ	Max	Unit
Specifications Guaranteed		25		°C
Functionality Guaranteed	–40		+85	°C
Storage	–65		+150	°C

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C, unless otherwise noted.)

AV_{DD}, DV_{DD}, OV_{DD} to AGND, DGND . . . –0.3 V to +6.0 V
AGND to DGND . . . . –0.3 V to +0.3 V
Digital I/O Voltage to DGND . . . . –0.3 V to ODV_{DD} + 0.3 V
Analog I/O Voltage to AGND . . . . . . –0.3 V to AV_{DD} + 0.3 V
Operating Temperature Range
Industrial (A Version) . . . . –40°C to +85°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

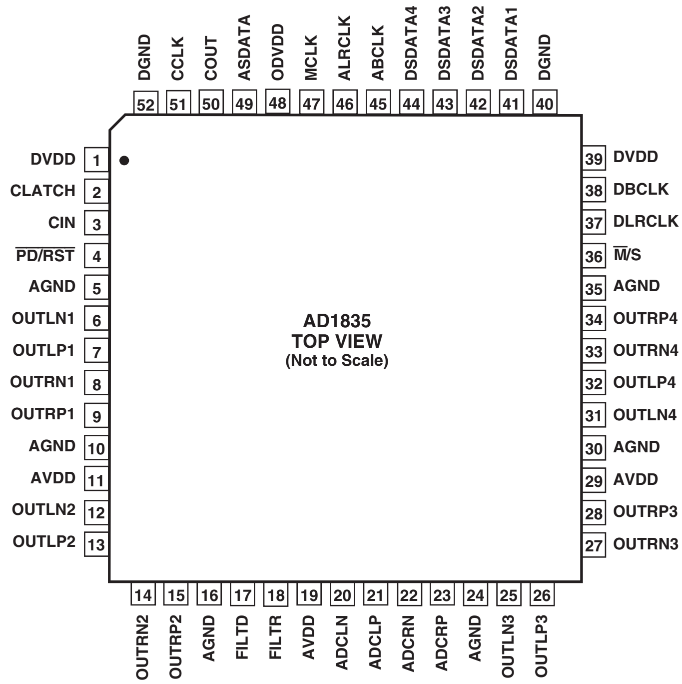
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD1835AS	–40°C to +85°C	52-Lead MQFP	S-52

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1835 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

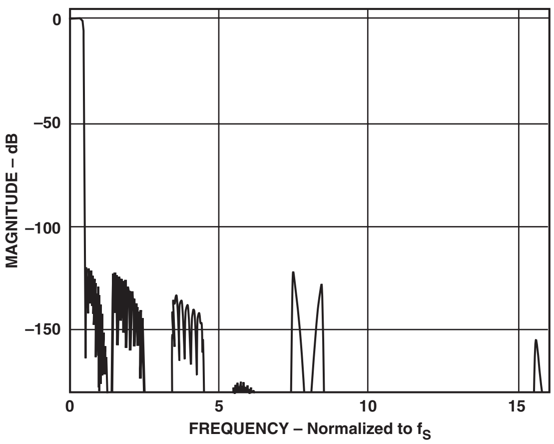
PIN CONFIGURATION



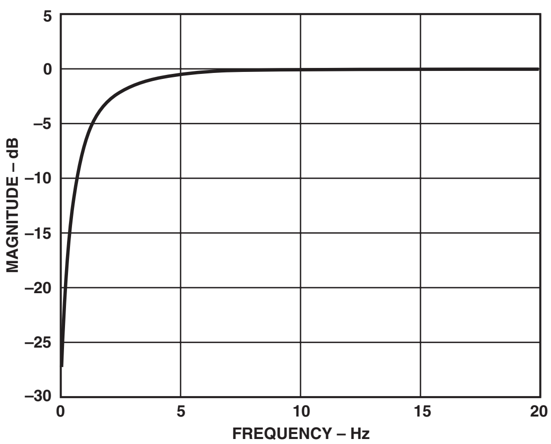
PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Input/ Output	Description
1, 39	DVDD		Digital Power Supply. Connect to digital 5 V supply.
2	CLATCH	I	Latch Input for Control Data
3	CIN	I	Serial Control Input
4	$\overline{\text{PD/RST}}$	I	Power-Down/Reset
5, 10, 16, 24, 30, 35	AGND		Analog Ground
6, 12, 25, 31	OUTLNx	O	DACx Left Channel Negative Output
7, 13, 26, 32	OUTLPx	O	DACx Left Channel Positive Output
8, 14, 27, 33	OUTRNx	O	DACx Right Channel Negative Output
9, 15, 28, 34	OUTRPx	O	DACx Right Channel Positive Output
11, 19, 29	AVDD		Analog Power Supply. Connect to analog 5 V supply.
17	FILTD		Filter Capacitor Connection. Recommended 10 μF 100 nF.
18	FILTR		Reference Filter Capacitor Connection. Recommended 10 μF 100 nF.
20	ADCLN	I	ADC Left Channel Negative Input
21	ADCLP	I	ADC Left Channel Positive Input
22	ADCRN	I	ADC Right Channel Negative Input
23	ADCRP	I	ADC Right Channel Positive Input
36	$\overline{\text{M}}$/S	I	ADC $\overline{\text{Master}}$/Slave Select
37	DLRCLK	I/O	DAC LR Clock
38	DBCLK	I/O	DAC Bit Clock
40, 52	DGND		Digital Ground
41–44	DSDATAx	I	DACx Input Data (Left and Right Channels)
45	ABCLK	I/O	ADC Bit Clock
46	ALRCLK	I/O	ADC LR Clock
47	MCLK	I	Master Clock Input
48	ODVDD		Digital Output Driver Power Supply
49	ASDATA	O	ADC Serial Data Output
50	COUT	O	Output for Control Data
51	CCLK	I	Control Clock Input for Control Data

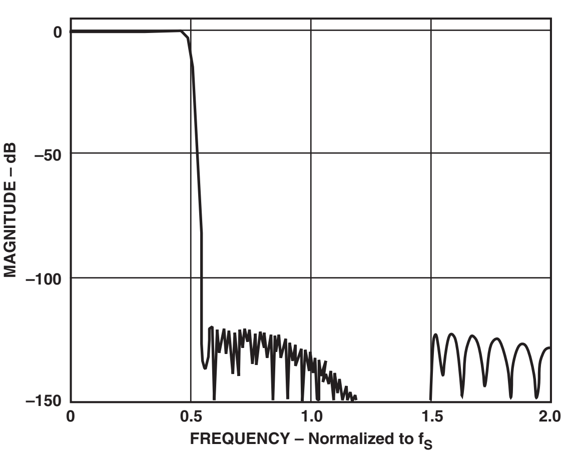
AD1835–Typical Performance Characteristics



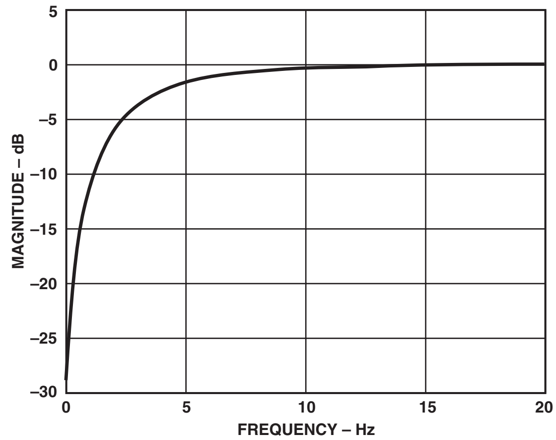
TPC 1. ADC Composite Filter Response



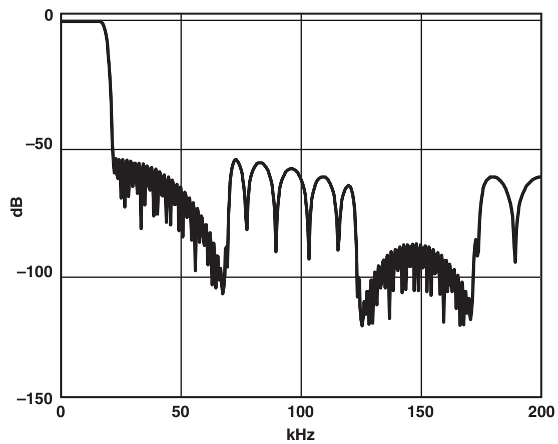
TPC 2. ADC High-Pass Filter Response, f_S = 48 kHz



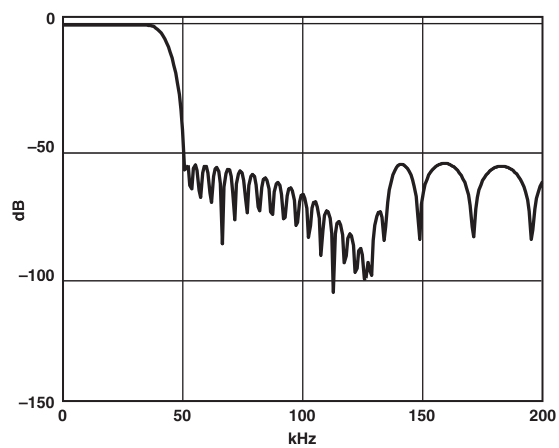
TPC 3. ADC Composite Filter Response (Pass-Band Section)



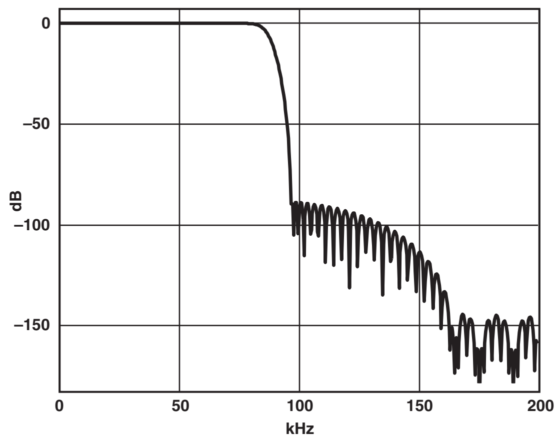
TPC 4. ADC High-Pass Filter Response, f_S = 96 kHz



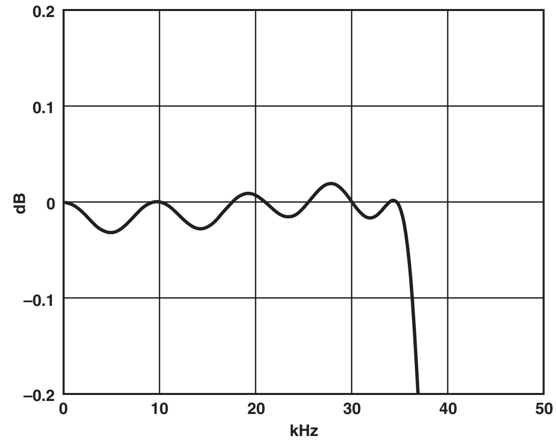
TPC 5. DAC Composite Filter Response, f_S = 48 kHz



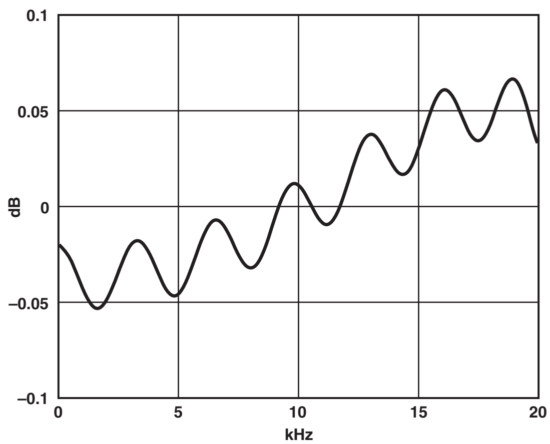
TPC 6. DAC Composite Filter Response, f_S = 96 kHz



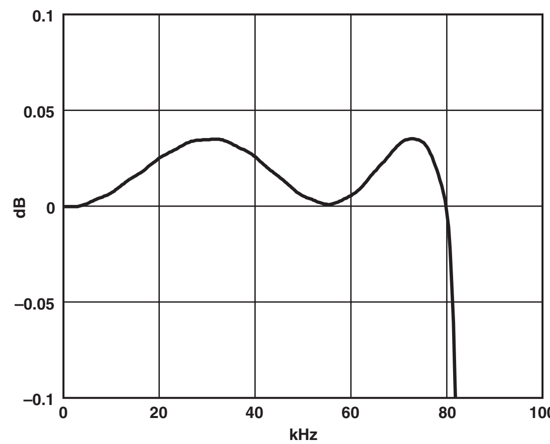
TPC 7. DAC Composite Filter Response, f_S = 192 kHz



TPC 9. DAC Composite Filter Response, f_S = 96 kHz (Pass-Band Section)



TPC 8. DAC Composite Filter Response, f_S = 48 kHz (Pass-Band Section)



TPC 10. DAC Composite Filter Response, f_S = 192 kHz (Pass-Band Section)

DEFINITIONS

Dynamic Range
The ratio of a full-scale input signal to the integrated input noise in the pass band (20 Hz to 20 kHz), expressed in decibels (dB). Dynamic range is measured with a –60 dB input signal and is equal to (S/[THD + N]) +60 dB. Note that spurious harmonics are below the noise with a –60 dB input, so the noise level establishes the dynamic range. The dynamic range is specified with and without an A-Weight filter applied.

Signal to (Total Harmonic Distortion + Noise) [S/(THD + N)]
The ratio of the root-mean-square (rms) value of the fundamental input signal to the rms sum of all other spectral components in the pass band, expressed in decibels (dB).

Pass Band
The region of the frequency spectrum unaffected by the attenuation of the digital decimator's filter.

Pass-Band Ripple
The peak-to-peak variation in amplitude response from equal-amplitude input signal frequencies within the pass band, expressed in decibels.

Stop Band
The region of the frequency spectrum attenuated by the digital decimator's filter to the degree specified by stop-band attenuation.

Gain Error
With a near full-scale input, the ratio of actual output to expected output, expressed as a percentage.

Interchannel Gain Mismatch
With identical near full-scale inputs, the ratio of outputs of the two stereo channels, expressed in decibels.

Gain Drift
Change in response to a near full-scale input with a change in temperature, expressed as parts-per-million (ppm) per °C.

Crosstalk (EIAJ Method)
Ratio of response on one channel with a grounded input to a full-scale 1 kHz sine wave input on the other channel, expressed in decibels.

Power Supply Rejection
With no analog input, signal present at the output when a 300 mV p-p signal is applied to power supply pins, expressed in decibels of full scale.

Group Delay
Intuitively, the time interval required for an input pulse to appear at the converter's output, expressed in milliseconds (ms). More precisely, the derivative of radian phase with respect to radian frequency at a given frequency.

Group Delay Variation
The difference in group delays at different input frequencies. Specified as the difference between the largest and the smallest group delays in the pass band, expressed in microseconds (μs).

GLOSSARY

ADC–Analog-to-Digital Converter

DAC–Digital-to-Analog Converter

DSP–Digital Signal Processor

IMCLK–Internal Master Clock signal used to clock the ADC and DAC engines

MCLK–External Master Clock signal applied to the AD1835

(Continued from Page 1)

and a continuous-time voltage out analog section. Each DAC has independent volume control and clickless mute functions. The ADC comprises two 24-bit conversion channels with multibit sigma-delta modulators and decimation filters.

The AD1835 also contains an on-chip reference with a nominal value of 2.25 V.

The AD1835 contains a flexible serial interface that allows for glueless connection to a variety of DSP chips, AES/EBU receivers, and sample rate converters. The AD1835 can be configured in Left-Justified, Right-Justified, I^2S-, or DSP-compatible serial modes. Control of the AD1835 is achieved by means of an SPI-compatible serial port. While the AD1835 can be operated from a single 5 V supply, it also features a separate supply pin for its digital interface that allows the device to be interfaced to other devices using 3.3 V power supplies.

The AD1835 is available in a 52-lead MQFP package and is specified for the industrial temperature range of –40°C to +85°C.

FUNCTIONAL OVERVIEW

ADCs

There are two ADC channels in the AD1835, configured as a stereo pair. Each ADC has fully differential inputs. The ADC section can operate at a sample rate of up to 96 kHz. The ADCs include on-board digital decimation filters with 120 dB stop-band attenuation and linear phase response, operating at an oversampling ratio of 128 (for 48 kHz operation) or 64 (for 96 kHz operation).

ADC peak level information for each ADC may be read from the ADC Peak 0 and ADC Peak 1 Registers. The data is supplied as a 6-bit word with a maximum range of 0 dB to –63 dB and a resolution of 1 dB. The registers will hold peak information until read; after reading, the registers are reset so that new peak information can be acquired. Refer to the register description for details on the format. The two ADC channels have a common serial bit clock and a left-right framing clock. The clock signals are all synchronous with the sample rate.

The ADC digital pins, ABCLK and ALRCLK, can be set to operate as inputs or outputs by connecting the $\overline{M}$/S pin to ODVDD or DGND, respectively. When the pins are set as outputs, the AD1835 will generate the timing signals. When the pins are set as inputs, the timing must be generated by the external audio controller.

DACs

The AD1835 has eight DAC channels arranged as four independent stereo pairs, with eight fully differential analog outputs for improved noise and distortion performance. Each channel has its own independently programmable attenuator, adjustable in 1024 linear steps. Digital inputs are supplied through four serial data input pins (one for each stereo pair) and a common frame (DLRCLK) and bit (DBLCK) clock. Alternatively, one of the "packed data" modes may be used to access all eight channels on a single TDM data pin. A stereo replicate feature is included where the DAC data sent to the first DAC pair is also sent to the other DACs in the part. The AD1835 can accept DAC data at a sample rate of 192 kHz on DAC 1 only. The stereo replicate feature can then be used to copy the audio data to the other DACs.

Each set of differential output pins sits at a dc level of V_{REF} and swings ±1.4 V for a 0 dB digital input signal. A single op amp third order external low-pass filter is recommended to remove high-frequency noise present on the output pins, as well as to provide differential-to-single-ended conversion. Note that the use of op amps with low slew rate or low bandwidth may cause high-frequency noise and tones to fold down into the audio band; care should be exercised in selecting these components.

The FILTD pin should be connected to an external grounded capacitor. This pin is used to reduce the noise of the internal DAC bias circuitry, thereby reducing the DAC output noise. In some cases, this capacitor may be eliminated with little effect on performance.

DAC and ADC Coding

The DAC and ADC output data stream is in a two's complement encoded format. The word width can be selected from 16-bit, 20-bit, or 24-bit. The coding scheme is detailed in Table I.

Table I. Coding Scheme

Code	Level
01111......1111	+FS
00000......0000	0 (Ref Level)
10000......0000	–FS

Clock Signals

The DAC and ADC engines in the AD1835 are designed to operate from a 24.576 MHz internal master clock (IMCLK). This clock is used to generate 48 kHz and 96 kHz sampling on the ADC and 48 kHz, 96 kHz, and 192 kHz on the DAC, although the 192 kHz option is only available on one DAC pair. The stereo replicate feature can be used to copy this DAC data to the other DACs if required.

To facilitate the use of different MCLK values, the AD1835 provides a clock scaling feature. The MCLK scaler can be programmed via the SPI port to scale the MCLK by a factor of 1 (pass-through), 2 (doubling), or scaling by a factor of 2/3. The default setting of the MCLK scaler is 2, which will generate 48 kHz sampling from a 12.288 MHz MCLK. Additional sample rates can be achieved by changing the MCLK value. For example, the CD standard sampling frequency of 44.1 kHz can be achieved using an 11.2896 kHz MCLK. Figure 2 shows the internal configuration of the clock scaler and converter engines.

To maintain the highest performance possible, it is recommended that the clock jitter of the master clock signal be limited to less than 300 ps rms, measured using the edge-to-edge technique. Even at these levels, extra noise or tones may appear in the DAC outputs if the jitter spectrum contains large spectral peaks. It is highly recommended that the master clock be generated by an independent crystal oscillator. In addition, it is especially important that the clock signal should not be passed through an FPGA or other large digital chip before being applied to the AD1835. In most cases, this will induce clock jitter due to the fact that the clock signal is sharing common power and ground connections with other unrelated digital output signals.

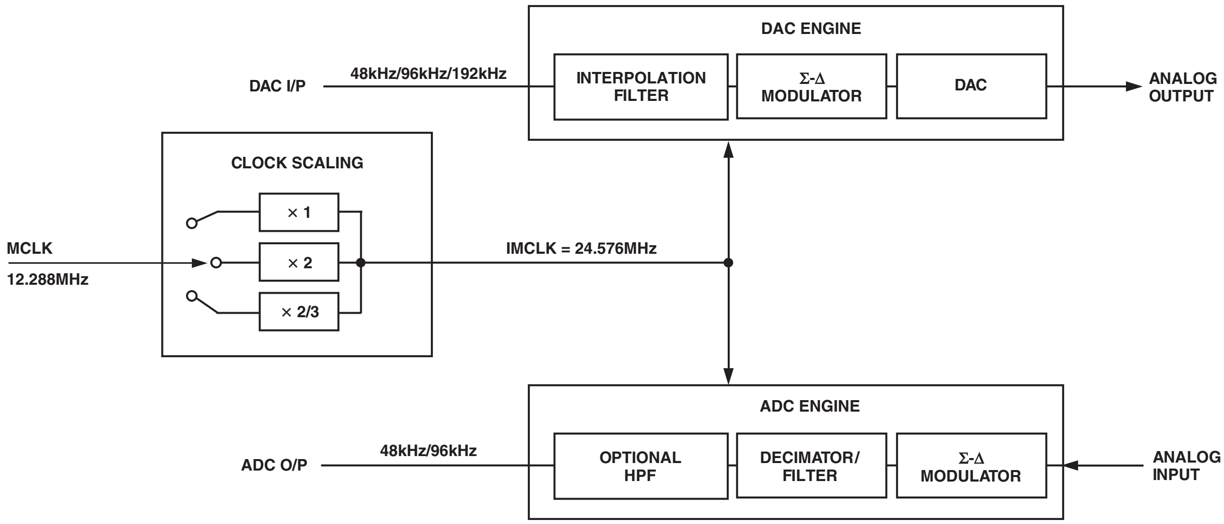


Figure 2. Modulator Clocking Scheme

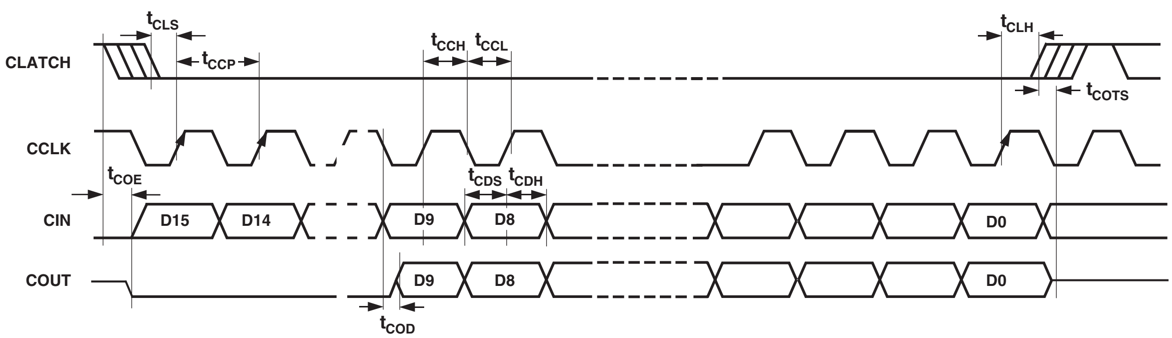


Figure 3. Format of SPI Timing

RESET and Power-Down

$\overline{PD/RST}$ will power down the chip and set the control registers to their default settings. After $\overline{PD/RST}$ is de-asserted, an initialization routine will run inside the AD1835 to clear all memories to zero. This initialization lasts for approximately 20 LRCLK intervals. During this time, it is recommended that no SPI writes occur.

Power Supply and Voltage Reference

The AD1835 is designed for 5 V supplies. Separate power supply pins are provided for the analog and digital sections. These pins should be bypassed with 100 nF ceramic chip capacitors, as close to the pins as possible, to minimize noise pickup. A bulk aluminum electrolytic capacitor of at least 22 µF should also be provided on the same PC board as the codec. For critical applications, improved performance will be obtained with separate supplies for the analog and digital sections. If this is not possible, it is recommended that the analog and digital supplies be isolated by means of two ferrite beads in series with the bypass capacitor of each supply. It is important that the analog supply be as clean as possible.

The internal voltage reference is brought out on the FILTR pin and should be bypassed as close as possible to the chip, with a parallel combination of 10 µF and 100 nF. The reference voltage may be used to bias external op amps to the common-mode voltage of the analog input and output signal pins. The current drawn from the V_{REF} pin should be limited to less than 50 µA.

Serial Control Port

The AD1835 has an SPI-compatible control port to permit programming the internal control registers for the ADCs and DACs and for reading the ADC signal levels from the internal peak detectors. The SPI control port is a 4-wire serial control port. The format is similar to the Motorola SPI format except the input data-word is 16 bits wide. The maximum serial bit clock frequency is 12.5 MHz and may be completely asynchronous to the sample rate of the ADCs and DACs. Figure 3 shows the format of the SPI signal.

Serial Data Ports—Data Format

The ADC serial data output mode defaults to the popular I^2S format, where the data is delayed by 1 BCLK interval from the edge of the LRCLK. By changing Bits 6 to 8 in ADC Control Register 2, the serial mode can be changed to Right-Justified (RJ), Left-Justified DSP (DSP), or Left-Justified (LJ). In the RJ mode, it is necessary to set Bits 4 and 5 to define the width of the data-word.

The DAC serial data input mode defaults to I²S. By changing Bits 5, 6, and 7 in DAC Control Register 1, the mode can be changed to RJ, DSP, LJ, Packed Mode 1, or Packed Mode 2. The word width defaults to 24 bits but can be changed by reprogramming Bits 3 and 4 in DAC Control Register 1.

Packed Modes

The AD1835 has a packed mode that allows a DSP or other controller to write to all DACs and read all ADCs using one input data pin and one output data pin. Packed Mode 256 refers to the number of BCLKs in each frame. The LRCLK is low while data from a left channel DAC or ADC is on the data pin and high while data from a right channel DAC or ADC is on the data pin. DAC data is applied on the DSDATA1 pin and ADC data is available on the ASDATA pin. Figures 7–10 show the timing for the packed mode. Packed mode is only available for 48 kHz and when the ADC is set as a master ($\overline{M}$/S = 0).

Auxiliary (TDM) Mode

A special auxiliary mode is provided to allow three external stereo ADCs to be interfaced to the AD1835 to provide 8-in/8-out operation. In addition, this mode supports glueless interface to a single SHARC DSP serial port, allowing a SHARC DSP to access all eight channels of analog I/O. In this special mode, many pins are redefined; see Table II for a list of redefined pins.

The auxiliary and the TDM interfaces are independently configurable to operate as masters or slaves. When the auxiliary interface is set as a master, by programming the Aux Mode bit in ADC Control Register II, the AUXLRCLK and AUXBCLK are generated by the AD1835. When the auxiliary interface is set as a slave, the AUXLRCLK and AUXBCLK need to be generated by an external ADC as shown in Figure 13.

The TDM interface can be set to operate as a master or slave by connecting the M/S pin to DGND or ODVDD, respectively. In master mode, the FSTDM and BCLK signals are outputs and generated by the AD1835. In slave mode, the FSTDM and BCLK are inputs and should be generated by the SHARC. Slave mode operation is available for 48 kHz and 96 kHz operation (based on a 12.288 MHz or 24.576 MHz MCLK) and master mode operation is available for 48 kHz only.

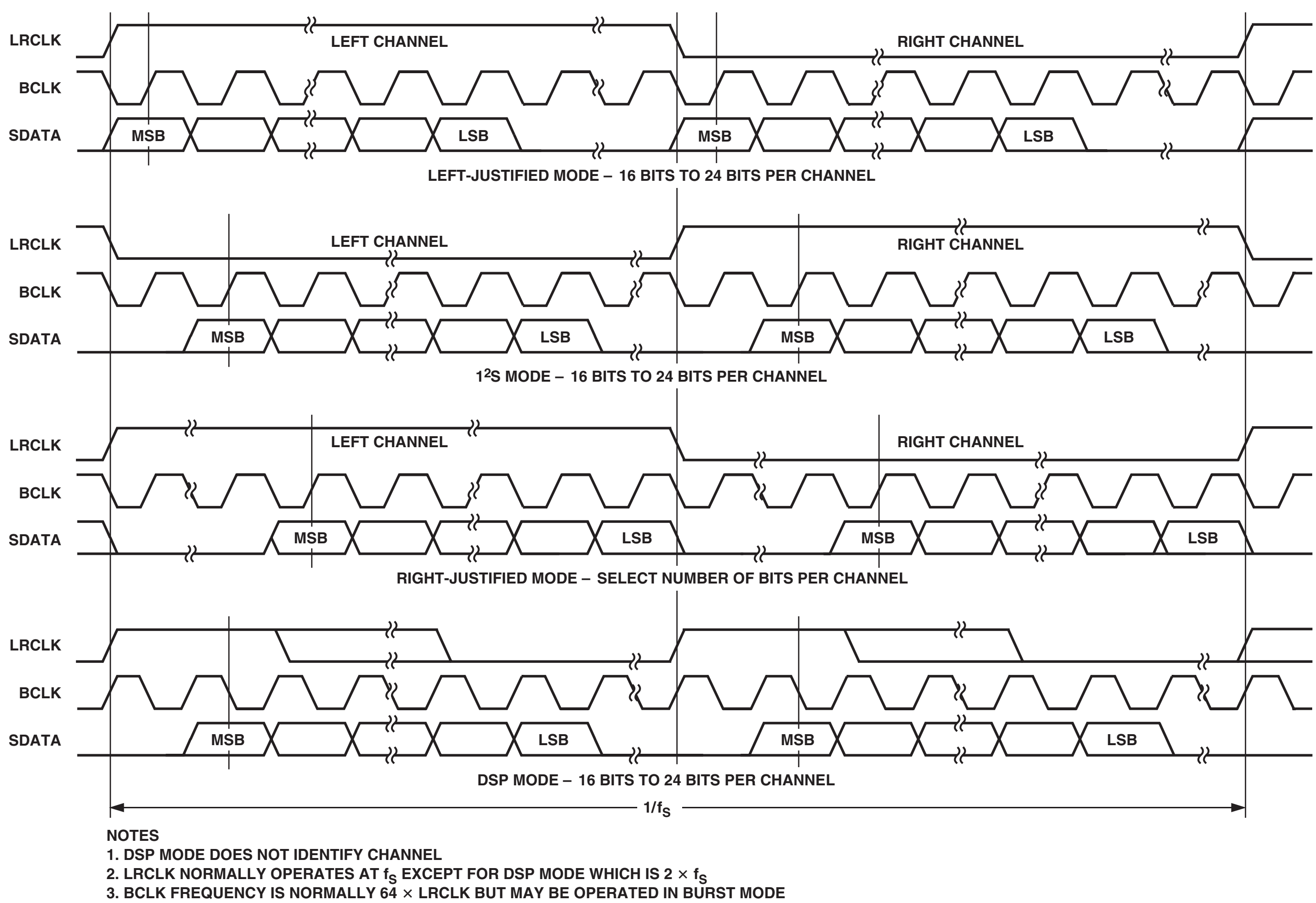


Figure 4. Stereo Serial Modes

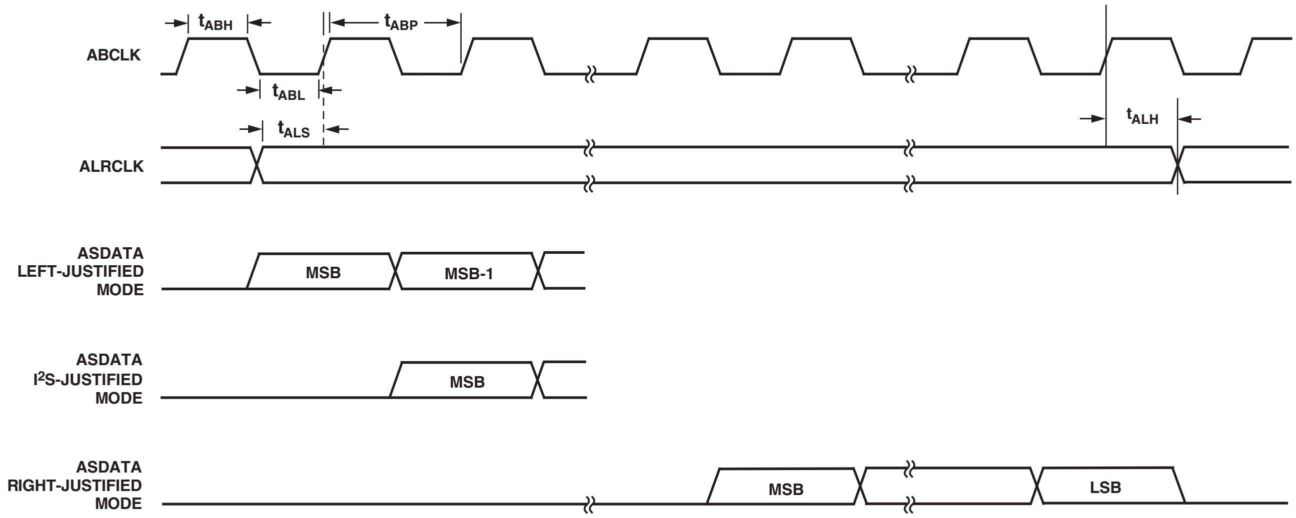


Figure 5. ADC Serial Mode Timing

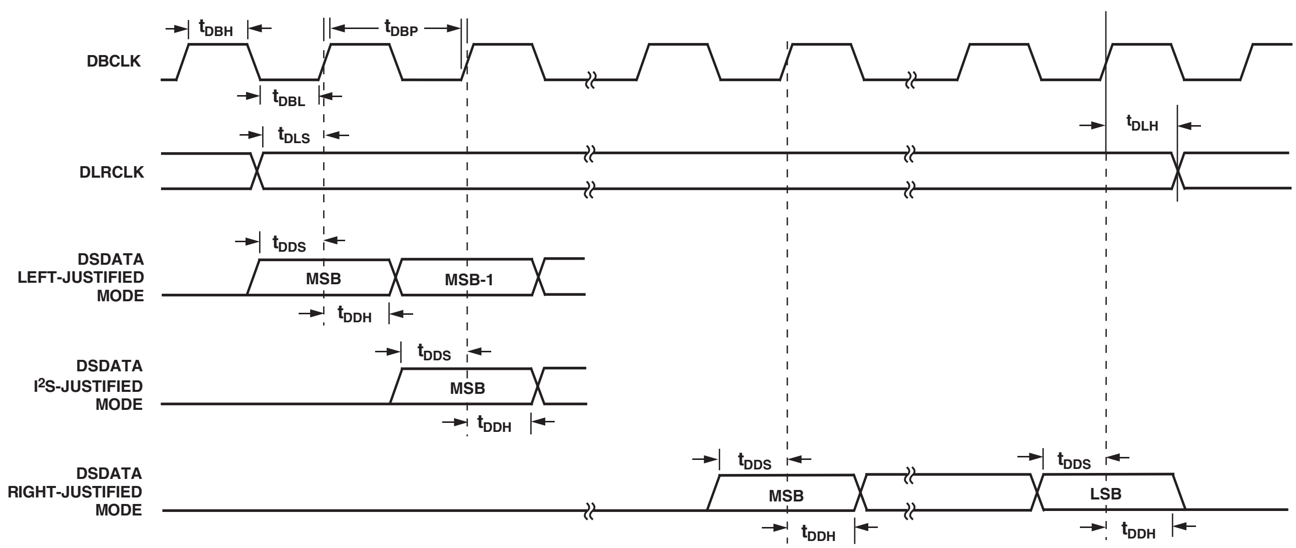


Figure 6. DAC Serial Mode Timing

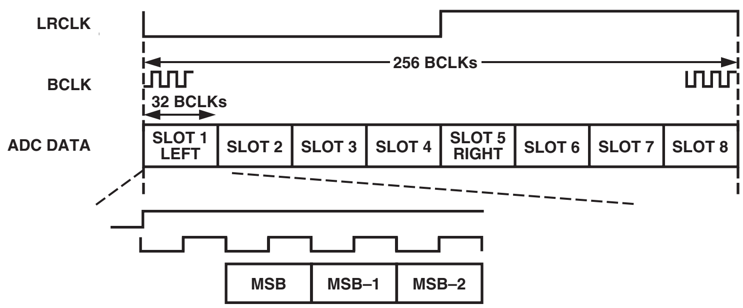


Figure 7. ADC Packed Mode 256

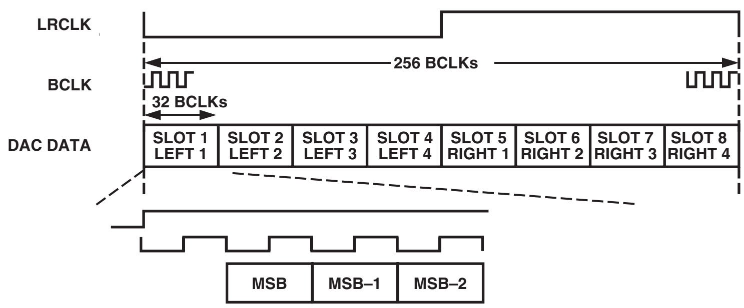


Figure 8. DAC Packed Mode 256

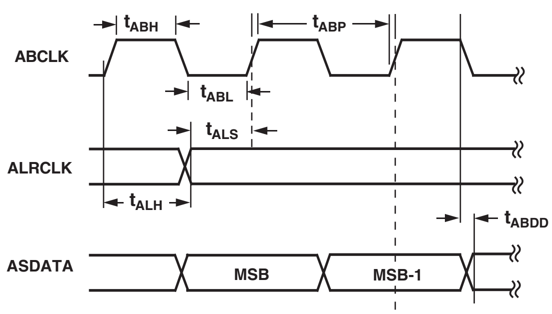


Figure 9. ADC Packed Mode Timing

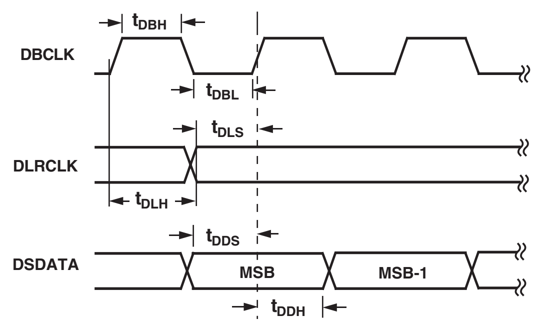


Figure 10. DAC Packed Mode Timing

Table II. Pin Function Changes in Auxiliary Mode

Pin Name	I^2S Mode	Aux Mode
ASDATA (O)	I^2S Data Out, Internal ADC	TDM Data Out to SHARC
DSDATA1 (I)	I^2S Data In, Internal DAC1	TDM Data In from SHARC
DSDATA2 (I)/AAUXDATA1 (I)	I^2S Data In, Internal DAC2	AUX-I^2S Data In 1 (from Ext. ADC)
DSDATA3 (I)/AAUXDATA2 (I)	I^2S Data In, Internal DAC3	AUX-I^2S Data In 2 (from Ext. ADC)
DSDATA4 (I)/AAUXDATA3 (I)	I^2S Data In, Internal DAC4	AUX-I^2S Data In 3 (from Ext. ADC)
ALRCLK (O)	LRCLK for ADC	TDM Frame Sync Out to SHARC
ABCLK (O)	BCLK for ADC	TDM BCLK Out to SHARC (FSTDM)
DLRCLK (I)/AUXLRCLK(I/O)	LRCLK In/Out Internal DACs	AUX LRCLK In/Out. Driven by Ext. LRCLK from ADC in slave mode. In master mode, driven by MCLK/512.
DBCLK (I)/AUXBCLK(I/O)	BCLK In/Out Internal DACs	AUX BCLK In/Out. Driven by Ext. BCLK from ADC in slave mode. In master mode, driven by MCLK/8.

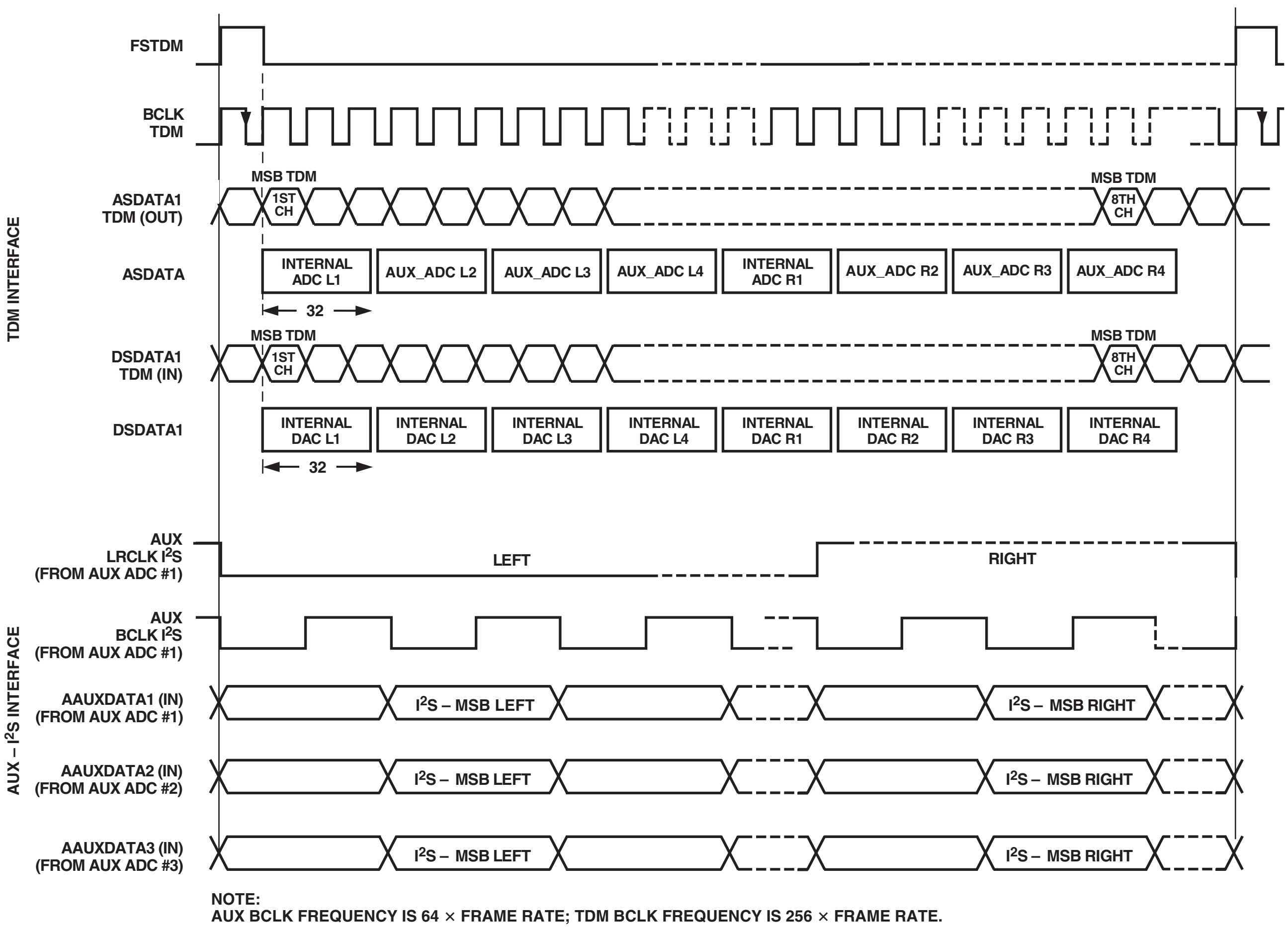


Figure 11. Aux Mode Timing

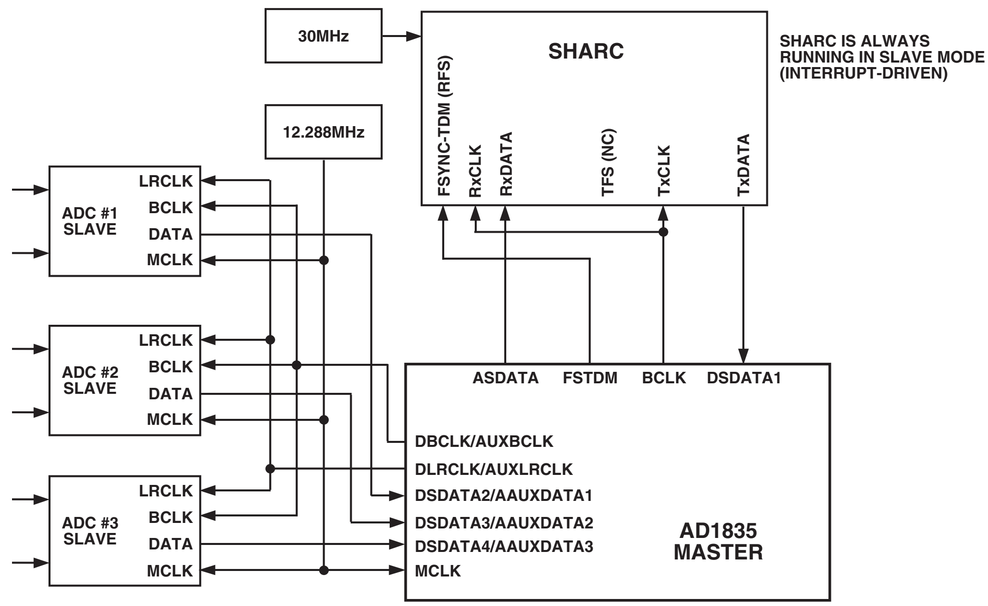


Figure 12. AUX-Mode Connection to SHARC (Master Mode)

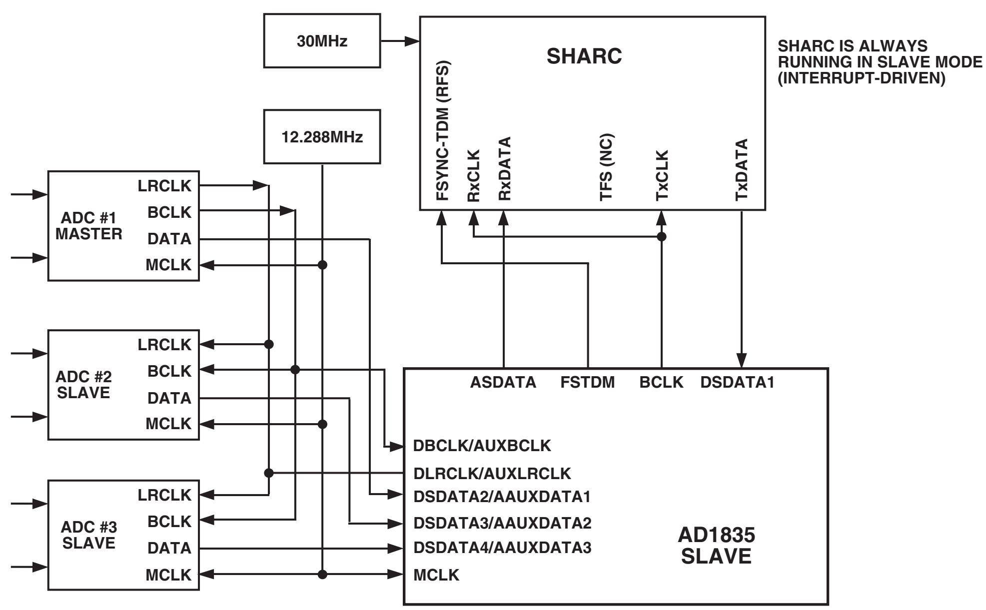


Figure 13. Aux Mode Connection to SHARC (Slave Mode)

CONTROL/STATUS REGISTERS

The AD1835 has 15 control registers, 13 of which are used to set the operating mode of the part. The other two registers, ADC Peak 0 and ADC Peak 1, are read-only and should not be programmed. Each of the registers is 10 bits wide with the exception of the ADC peak reading registers which are 6 bits wide. Writing to a control register requires a 16-bit data frame to be transmitted. Bits 15 to 12 are the address bits of the required register. Bit 11 is a read/write bit. Bit 10 is reserved and should always be programmed to 0. Bits 9 to 0 contain the 10-bit value that is to be written to the register or, in the case of a read operation, the 10-bit register contents. Figure 3 shows the format of the SPI read and write operation.

DAC Control Registers

The AD1835 register map has 10 registers that are used to control the functionality of the DAC section of the part. The function of the bits in these registers is discussed below.

Sample Rate

These bits control the sample rate of the DACs. Based on a 24.576 MHz IMCLK, sample rates of 48 kHz, 96 kHz, and 192 kHz are available. The MCLK scaling bits in ADC Control III should be programmed appropriately, based on the master clock frequency.

Power-Down/Reset

This bit controls the power-down status of the DAC section. By default normal mode is selected, but by setting this bit, the digital section of the DAC stage can be put into a low-power mode, thus reducing the digital current. The analog output section of the DAC stage is not powered down.

DAC Data-Word Width

These two bits set the word width of the DAC data. Compact Disc (CD) compatibility may require 16 bits, but many modern digital audio formats require 24-bit sample resolution.

DAC Data Format

The AD1835 serial data interface can be configured to be compatible with a choice of popular interface formats, including I^2S, LJ, RJ, or DSP modes. Details of these interface modes are given in the Serial Data Port section of this data sheet.

De-Emphasis

The AD1835 provides built-in de-emphasis filtering for the three standard samples rates of 32.0 kHz, 44.1 kHz, and 48 kHz.

Mute DAC

Each of the eight DACs in the AD1835 has its own independent mute control. Setting the appropriate bit will mute the DAC output. The AD1835 uses a clickless mute function that attenuates the output to approximately –100 dB over a number of cycles.

Stereo Replicate

Setting this bit copies the digital data sent to the stereo pair DAC1 to the three other stereo DACs in the system. This allows all four stereo DACs to be driven by one digital data stream. Note that in this mode DAC data sent to the other DACs is ignored.

DAC Volume Control

Each DAC in the AD1835 has its own independent volume control. The volume of each DAC can be adjusted in 1024 linear steps by programming the appropriate register. The default value for this register is 1023, which provides no attenuation, i.e., full volume.

ADC Control Registers

The AD1835 register map has five registers that are used to control the functionality and read the status of the ADCs. The function of the bits in each of these registers is discussed below.

ADC Peak Level

These two registers store the peak ADC result from each channel when the ADC peak readback function is enabled. The peak result is stored as a 6-bit number from 0 dB to –63 dB in 1 dB steps. The value contained in the register is reset once it has been read, allowing for continuous level adjustment as required. Note that the ADC peak level registers use the six most significant bits in the register to store the results.

Sample Rate

This bit controls the sample rate of the ADCs. Based on a 24.576 MHz IMCLK, sample rates of 48 kHz and 96 kHz are available. The MCLK scaling bits in ADC Control III should be programmed appropriately based on the master clock frequency.

ADC Power-Down

This bit controls the power-down status of the ADC section and operates in a similar manner to the DAC power-down.

High-Pass Filter

The ADC signal path has a digital high-pass filter. Enabling this filter will remove the effect of any dc offset in the analog input signal from the digital output codes.

Dither

Enabling the dither function will add a small amount of random charge to the sampling capacitors on the ADC inputs. This will eliminate the effect of any idle tones that could occur if there were no input signal present.

ADC Data-Word Width

These two bits set the word width of the ADC data.

ADC Data Format

The AD1835 serial data interface can be configured to be compatible with a choice of popular interface formats, including I^2S, LJ, RJ, or DSP modes.

Master/Slave Auxiliary Mode

When the AD1835 is operating in the auxiliary mode, the auxiliary ADC control pins, AUXBCLK and AUXLRCLK, that connect to the external ADCs, can be set to operate as a master or slave. If the pins are set in slave mode, one of the external ADCs should provide the LRCLK and BCLK signals.

ADC Peak Readback

Setting this bit enables ADC peak reading. See the ADC section for more information.

Table III. Control Register Map

Register Address	Register Name	Description	Type	Width	Reset Setting (Hex)
0000	DACCTRL1	DAC Control 1	R/$\overline{W}$	10	000
0001	DACCTRL2	DAC Control 2	R/$\overline{W}$	10	000
0010	DACVOL1	DAC Volume–Left 1	R/$\overline{W}$	10	3FF
0011	DACVOL2	DAC Volume–Right 1	R/$\overline{W}$	10	3FF
0100	DACVOL3	DAC Volume–Left 2	R/$\overline{W}$	10	3FF
0101	DACVOL4	DAC Volume–Right 2	R/$\overline{W}$	10	3FF
0110	DACVOL5	DAC Volume–Left 3	R/$\overline{W}$	10	3FF
0111	DACVOL6	DAC Volume–Right 3	R/$\overline{W}$	10	3FF
1000	DACVOL7	DAC Volume–Left 4	R/$\overline{W}$	10	3FF
1001	DACVOL8	DAC Volume–Right 4	R/$\overline{W}$	10	3FF
1010	ADCPeak0	ADC Left Peak	R	6	000
1011	ADCPeak1	ADC Right Peak	R	6	000
1100	ADCCTRL1	ADC Control 1	R/$\overline{W}$	10	000
1101	ADCCTRL2	ADC Control 2	R/$\overline{W}$	10	000
1110	ADCCTRL3	ADC Control 3	R/$\overline{W}$	10	000
1111	Reserved	Reserved	R/$\overline{W}$	10	Reserved

Table IV. DAC Control I

			FUNCTION				
Address	R/$\overline{W}$	RES	De-Emphasis	DAC Data Format	DAC Data-Word Width	Power-Down Reset	Sample Rate
15, 14, 13, 12	11	10	9, 8	7, 6, 5	4, 3	2	1, 0
0000	0	0	00 = None 01 = 44.1 kHz 10 = 32.0 kHz 11 = 48.0 kHz	000 = I^2S 001 = RJ 010 = DSP 011 = LJ 100 = Pack Mode 256 101 = Reserved 110 = Reserved 111 = Reserved	00 = 24 Bits 01 = 20 Bits 10 = 16 Bits 11 = Reserved	0 = Normal 1 = Power-Down	00 = 8 × (48 kHz) 01 = 4 × (96 kHz) 10 = 2 × (192 kHz) 11 = 8 × (48 kHz)

Table V. DAC Control II

				FUNCTION								
					MUTE DAC							
Address	R/$\overline{W}$	RES	Reserved	Stereo Replicate	OUTR4	OUTL4	OUTR3	OUTL3	OUTR2	OUTL2	OUTR1	OUTL1
15, 14, 13, 12	11	10	9	8	7	6	5	4	3	2	1	0
0001	0	0	0	0 = Off 1 = Replicate	0 = On 1 = Mute	0 = On 1 = Mute	0 = On 1 = Mute	0 = On 1 = Mute	0 = On 1 = Mute	0 = On 1 = Mute	0 = On 1 = Mute	0 = On 1 = Mute

Table VI. DAC Volume Control

Address	R/$\overline{W}$	RES	FUNCTION DAC Volume
15, 14, 13, 12	11	10	9, 8, 7, 6, 5, 4, 3, 2, 1, 0
0010 = DACL1 0011 = DACR1 0100 = DACL2 0101 = DACR2 0110 = DACL3 0111 = DACR3 1000 = DACL4 1001 = DACR4	0	0	0000000000 = 1/1024 0000000001 = 2/1024 0000000010 = 3/1024 1111111110 = 1022/1024 1111111111 = 1023/1024

Table VII. ADC Peak

Address	R/W	RES	FUNCTION Six Data Bits	 Four Fixed Bits
15, 14, 13, 12	11	10	9, 8, 7, 6, 5, 4	3, 2, 1, 0
0010 = Left ADC 1011 = Right ADC	1	0	000000 = 0.0 dBFS 000001 = –1.0 dBFS 000010 = –2.0 dBFS 111111 = –63.0 dBFS	0000 These four bits are always zero

Table VIII. ADC Control I

Address	R/$\overline{W}$	RES	FUNCTION Dither	 Filter	 ADC Power-Down	 Sample Rate	 Reserved
15, 14, 13, 12	11	10	9	8	7	6	5, 4, 3, 2, 1, 0
1100	0	0	0 = Disabled 1 = Enabled	0 = All Pass 1 = High-Pass	0 = Normal 1 = Power-Down	0 = 48 kHz 1 = 96 kHz	0, 0, 0, 0, 0, 0 0, 0, 0, 0, 0, 0

Table IX. ADC Control II

Address	R/$\overline{W}$ RES	RES	FUNCTION Master/Slave Aux Mode	 ADC Data Format	 ADC Data-Word Width	 Reserved	ADC MUTE Right	 Left
15, 14, 13, 12	11	10	9	8, 7, 6	5, 4	3, 2	1	0
1101	0	0	0 = Slave 1 = Master	000 = I^2S 001 = RJ 010 = DSP 011 = LJ 100 = Packed 256 101 = Reserved 110 = Auxiliary 256 111 = Auxiliary 512	00 = 24 Bits 01 = 20 Bits 10 = 16 Bits 11 = Reserved	0, 0	0 = On 1 = Mute	0 = On 1 = Mute

Table X. ADC Control III

Address	R/$\overline{W}$ RES	RES	FUNCTION Reserved	 IMCLK Clocking Scaling	 ADC Peak Readback	 DAC Test Mode	 ADC Test Mode
15, 14, 13, 12	11	10	9, 8	7, 6	5	4, 3, 2	1, 0
1110	0	0	0, 0	00 = MCLK × 2 01 = MCLK 10 = MCLK × 2/3 11 = MCLK × 2	0 = Disabled Peak Readback 1 = Enabled Peak Readback	000 = Normal Mode All others reserved	00 = Normal Mode All others reserved

CASCADE MODE

Dual AD1835Cascade

The AD1835 can be cascaded to an additional AD1835 that, in addition to six external stereo ADCs, can be used to create a 32-channel audio system with 16 inputs and 16 outputs. The cascade is designed to connect to a SHARC DSP and operates in a time division multiplexing (TDM) format. Figure 14 shows the connection diagram for cascade operation. The digital interface for both parts must be set to operate in Auxiliary 512 mode by programming ADC Control Register II. AD1835 #1 is set as a master device by connecting the $\overline{M}$/S pin to DGND, and AD1835 #2 is set as a slave device by connecting the $\overline{M}$/S to DVDD. Both devices should be run from the same MCLK and $\overline{PD/RST}$ signals to ensure that they are synchronized.

With Device 1 set as a master, it will generate the frame-sync and bit clock signals. These signals are sent to the SHARC and Device 2 ensuring that both know when to send and receive data.

The cascade can be thought of as two 256-bit shift registers, one for each device. At the beginning of a sample interval, the shift registers contain the ADC results from the previous sample interval. The first shift register (Device 1) clocks data into the SHARC and also clocks in data from the second shift register (Device 2). While this is happening, the SHARC is sending DAC data to the second shift register. By the end of the sample interval, all 512 bits of ADC data in the shift registers will have been clocked into the SHARC and been replaced by DAC data which is subsequently written to the DACs. Figure 15 shows the timing diagram for the cascade operation.

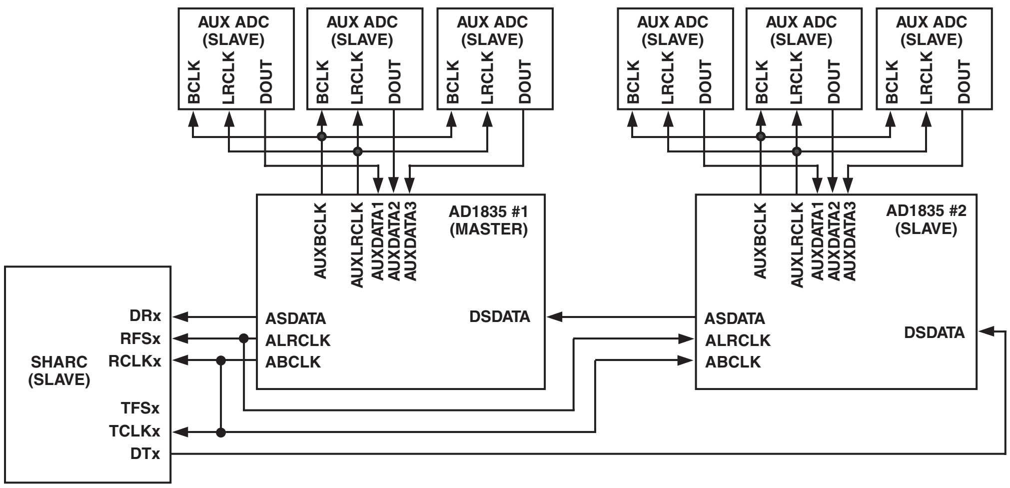


Figure 14. Cascade

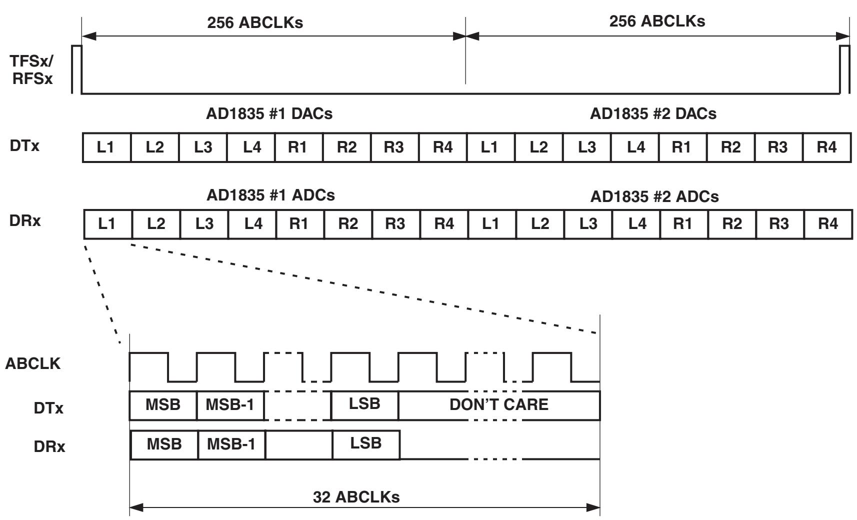


Figure 15. Cascade Timing

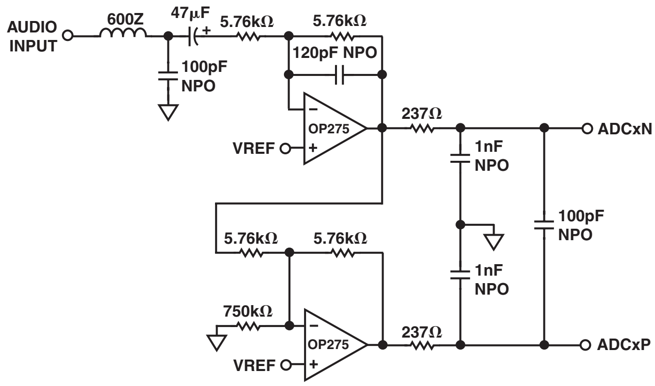


Figure 16. Typical ADC Input Filter Circuit

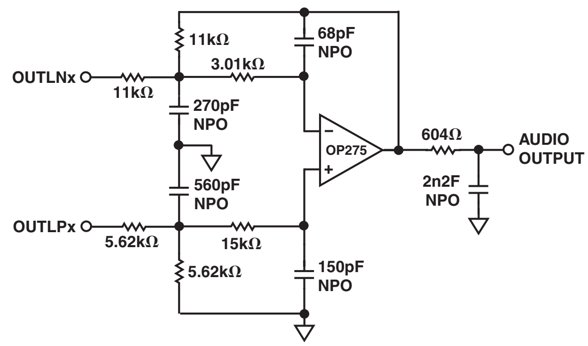


Figure 17. Typical DAC Output Filter Circuit

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

52-Lead MQFP
(S-52)