0.35μ Standard Cell

Application

Flextronics Semiconductor's 0.35μ Standard Cell product suite offers designers the best optimization for 3.3 voltage performance and power. Applications benefiting from these features are telecom, networking, portable datacom, and consumer applications. The product suite is well equipped for design teams who intend to migrate from advanced FPGA to full system on chip ASIC as well as system architects who need to prototype with an ASIC. Production is "all about results" utilizing Flextronics manufacturing supply chain muscle to execute cycle-time and cost performance.

Description

Sub-micron CMOS silicon utilizing a 0.32μ effective gate length capable of up to 125 MHz operation and 4.5 M logic gates.

Low power 3.3 volt core operation with 0.2 μW/gate/MHz power dissipation.

Dense, fast SRAM memory compilers and instances.

Low noise 3.3V and 3.3V with 5.0V tolerant I/O library designed for minimum die size / performance utilizing staggered and in-line configurations. Complete pad sets tested for 2 kV (HBM) ESD and 100 mA latchup.

Process	
Core Voltage	3.3 V
I/O Voltage	3.3 V operation 5.0 V tolerant
Poly/Metal Density	1P5M (20K gates/mm^2)
Power Dissipation	0.2 μW/gate/MHz

Standard Cell	Over 450 cells engineered for optimum synthesis and high routability.
I/O Functions	300+ CMOS/TTL functions with multiple drive strengths (1 mA to 24 mA) 3.3V and (1 mA to 6 mA) 5V tolerant. The 5V tolerant function requires no external bias pin.
Application Specific I/O	PCI, PECL, GTL, USB, LVDS, POR Clock driver; crystal oscillator; analog input; power, ground, & spacer cells for SoC compatibility.
SRAM / 1P	Single port SRAM compiler is a high density, high performance solution for embedded applications. Six transistor bordered bit cells achieve reduced die area while maintaining low tooling (mask) cost. The compiler maintains multi-bank architecture with capacity up to 576 Kbits.
SRAM / DP	High density dual port SRAM compiler offers a high performance solution with the highest density for embedded memory applications. Eight transistor bordered bit cells achieve minimum die area while maintaining low tooling (mask) cost. The compiler maintains multi-bank architecture with capacity up to 576 Kbits.
PLL	Programmable PLL with external divider allows designers to create a customized PLL for clock management in the system design.
Frequency Synthesizer	Sophisticated frequency synthesizer targeted for applications such as pixel (dot clock) generation for use as a video master and non-integer clock multiplication for high-speed networking application. Cascaded PLL architecture for precision & phase jitter stability.

Design Kit Support

EDA views	Verilog views with best case and worse case timing and typical case power data
	VHDL views with best case and worse case timing and typical case power data
	Synopsys views with best case and worse case timing and typical case power data

Our design kits include a broad selection of embedded semiconductor intellectual property components including standard cell logic, standard I/O, specialty I/O interfaces, memory, and PLL options. System on chip options include bus standards, connectivity standards, high speed serial I/O, cryptology, and applied FEC applications. Please contact us regarding your specific requirements.

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