FLEXTRONICS Semiconductor

PRELIMINARY DATA SHEET

0.13µ Standard Cell

Application

Flextronics Semiconductor's 0.13µ Standard Cell product suite offer designers the best high-volume solution for 3.3V performance, low power, and system cost. Applications benefiting from these features are telecom, networking, portable datacom, and consumer applications. The product suite is well equipped for design teams who intend to migrate from advanced FPGA to full system on chip ASIC as well as system architects who need to prototype with an ASIC. Production is "all about results" utilizing Flextronics manufacturing supply chain muscle to execute cycle-time and cost performance.

Description

Deep sub-micron CMOS silicon utilizing a 0.09µ effective gate length capable of up to 600 MHz operation and 88M logic gates.

Low power 1.2 volt core operation with 0.01 µW/gate/MHz power dissipation.

Dense, fast SRAM, and Multi-port Register File compilers and instance options up to 1Mbit.

High Density fully diffused ROM compiler up to 1Mbit.

Low noise 3.3 v /O library designed for minimum die size / performance utilizing staggered, in-line, and flip-chip configurations. Complete pad sets tested for 4000 volts ESD and 300 ma latchup.

Process	
Core Voltage	1.2 V
I/O Voltage	3.3 V operation
Poly/Metal Density	1P8M (220K gates/mm^2)
Power Dissipation	0.01 µW/gate/MHz

Features	
Standard Cells	550+ cell engineered for optimum synthesis and high routability.
High Performance Logic Cells	400+ high speed cells optimized for performance applications.
I/O Functions	400+ CMOS/TTL functions with multiple drive strengths (2 ma to 16 ma) 3.3 v with built in level shifters.
Application Specific I/O	PCI, PCI-X, SSTL, SSTL_2, HSTL, USB, LVDS Clock driver, crystal oscillator, analog input, power, ground, and spacer cells for SoC compatibility.
SRAM / SP	Single port SRAM compiler is a high density, high performance solution for embedded applications. Six transistor borderless bit cells achieve reduced die area while maintaining low tooling (mask) cost. The compilier maintains multi-bank architecture with capacity up to 1 Mbit.
SRAM / DP	High density dual port SRAM compiler offers a high performance solution with the highest density for embedded memory applications. Eight transistor bordered bit cells achieve minimum die area while maintaining low tooling (mask) cost. The compiler maintains multi-bank architecture with capacity up to 256 Kbit.

	Features (continued)
SRAM / 2P	Register compiled high performance two port memory solution for embedded applications. Best solution for register files, buffer memories, fall-through FIFO, palette RAM, and tag RAM. Capacity to compile very wide words up to 144 bits for address matching and virtual address. Low overhead of decode-logic and sense amplifiers minimize required die area.
ROM	Read Only Memory compiler is a high density, fully diffused ROM solution targeted for embedded applications that require program store. The bit cells are optimized to offer very high density and low power. Configurations up to 1 Mbit are available. Metal programmable versions are also available on a custom basis.
PLL	Compiler based technology that allows system designers to choose the center frequency, duty cycle, and create a customized PLL. Fully modular and embedded in the I/O pad ring with no area overhead to the core – eliminates manual wiring of analog power supply or additional band-gaps / external components.
Frequency Synthesizer	Sophisticated frequency synthesizer targeted for applications such as pixel (dot clock) generation for use a s a video master and non-integer clock multiplication for high-speed networking application. Cascaded PLL architecture for precision and phase jitter stability. Fully modular and embedded in the I/O pad ring with no area overhead to the core – eliminates manual wiring of analog power supply or additional band-gaps / external components.
Design Kit Support	
EDA views	Verilog views with best case and worse case timing and power data VHDL views with best case and worse case timing and power data Synopsys views with best case and worse case timing and power data

Our design kits include a broad selection of embedded semiconductor intellectual property components including standard cell logic, standard I/O, specialty I/O interfaces, memory, and PLL options. Please contact us regarding your specific requirements.

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